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ECL/CAMAC Trigger Processor System Documentation

Prepared by

E. Barsotti, J. Appel, S. Bracker,* M. Haldeman,

R. Hance, B. Haynes, D. Kline, J. Krebs,

J. Maenpaa, T. Nash, T. Soszynski

and K. Treptow

Fermi National Accelerator Laboratory

Batavia, Illinois 60510

*University of Toronto, Ontario, Canada

Introduction

This Technical Memo is a compendium of detailed documentaion for the ECL-Camac Trigger Processing System. It is intended for those interested in using this system and requiring more information after having read Fermilab Technical Memo 823, A Modular Trigger Processing System for High Energy Physics Experiments, which is available as a preprint and which will be published in the Proceedings of the October 1978 IEEE Nuclear Science Symposium.

At the end of most sections is a list of drawing numbers, software, etc. that is available to those wishing to duplicate a particular design. This material may be obtained by writing to Mr. J. Krebs or Mrs. L. Hanabarger, Research Services Department, Fermilab. Technical questions may be addressed to E. Barsotti or T. Nash at Fermilab.

Software, including that necessary to test modules and subsystems and to load memories, is available or under preparation. Documentation will be included in future editions of this Technical Memo. The software is written for use on a PDP11. It will allow users to write subroutines in Fortran defining the memory load for a given MLU (ECL2) without detailed knowledge of the inner workings of the module, the ordering of parameters in the input or output fields, or the location and memory configuration of the module. Information of this sort should be placed in a Configuration File on disk which is referenced by

the software and which may be written on tape at the beginning of each run, for example. This file defines the complete detailed configuration of a processor at any given time. Reference to this file and appropriate software commands will allow full, automatic, system simulation to test hardware.

We would like to thank Mary Luba for typing all of this documentation.

E516 TRIGGER PROCESSOR COOLING

The heat from the crates and power supplies used in the trigger processor is removed by the passage of air through these units. Four different interface units are used to build a cooling configuration. Interface units adapt fans, crate power supplies, and baffles to one another as well as crate to crate combinations. The configuration should in general be based on the fact that the exhaust temperature from any unit should not exceed 60^{o} C.

Although many more possible interface configurations exist, the most desirable are listed in the interface selection table (Table I). This table indicates what is required to build or modify a configuration. The table is used as follows: If one decides to place a fan above a crate (the fan is the upper unit, the crate being the lower unit) look for the intersection of the row labeled "crate (top)" and the column labeled "fan (intake)". The intersection indicates interface module "A" is required between the crate and the fan.

Using this procedure it becomes obvious that a power supply over a crate requires interface units A and D, where as a crate over a power supply requires interface unit D only.

Going one step farther one can write out combinations with air flow following the arrows as follows;

C → CR → A → F → D → PS → D → C

where D = power supply adapter

CR = crate

C = air intake or exhaust baffel

A = crate top adapter

F = fan unit

PS = power supply.

Preliminary tests were made, with the power supply dissipating approximately 300 watts, using the configuration shown in Fig. 1. The exhaust air temperature rise with the fan off and on was 16.6^{o} C and 4.3^{o} C respectively.

A similar measurement was made with a crate using the configuration of Fig. 2. In figures 1 and 2 the air intake is shown below the cooled unit; it may also be turned over and placed above the fan (no interface required; see table) as an air exhaust.

A crate full of modules with a total heat dissipation of approximately 700 watts was simulated. The exhaust air temperature rise for the fan off and on was 13^{o} C and 4.5^{o} C respectively.

At present the cooling interface modules are being made as well as other equipment and the above measurements are mentioned here only to give a very rough estimate of what may be expected.

Naturally power supplies as well as crates may be stacked with no fan or a fan below, between, or above them. Many possibilities exist and depend on individual situations.

The initial configuration used for E516 going from bottom toward the top of the equipment rack (i.e. the direction of air flow) is:

PS → D → F → C → PS → D → F → C → CR → A → F → C
→ CR → A → F → C → NIMBIN

where

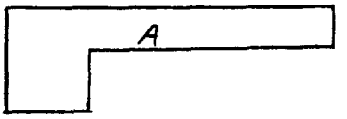
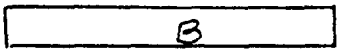
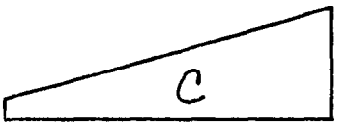
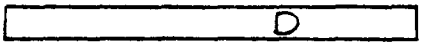
PS = power supply
D = power supply adapter
F = fan unit
C = exhaust baffel (out rack front)
CR = crate
A = crate top adapter

This is shown in Drwg. no. 0880-MC-104554.

(Prepared by M. Haldeman, P. Rowson)

TABLE I

COOLING SYSTEM INTERFACE UNITS

INTERFACE UNIT	INTERFACE UNIT OUTLINE (SIDE VIEW)	DRAWING NUMBER
CRATE TOP		0880-MC-104525
CRATE BOTTOM		0880-MD-104526
AIR INTAKE OR EXHAUST BAFFEL		0880-MC-104527
POWER SUPPLY TOP OR BOTTOM		0880-MC-104524

INTERFACE SELECTION TABLE

LOWER UNIT \ UPPER UNIT	FAN (INTAKE) *	POWER SUPPLY (BOTTOM)	CRATE (BOTTOM)	C
FAN (EXHAUST) *	NONE	D	B	NONE
POWER SUPPLY (TOP)	D	NONE	D	D
CRATE (TOP)	A	A AND D	A	A
C	NONE	D	NONE	NONE

* ASTRO DYNAMICS MODEL 5106 AIRE-AMPLIFIER

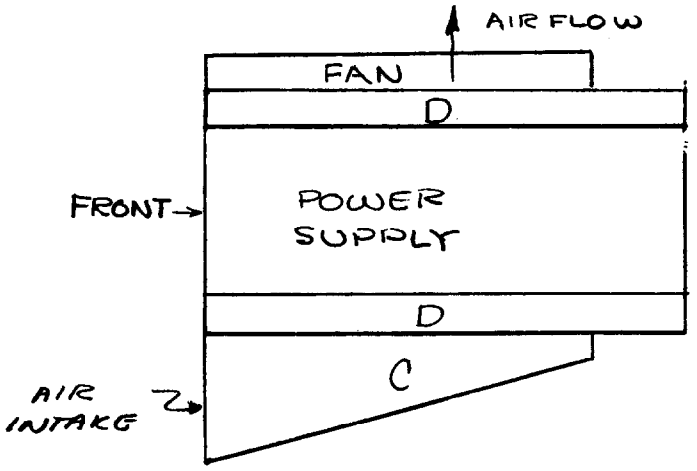

AIR FLOW
FAN
D
FRONT
POWER SUPPLY
D
C
AIR INTAKE

FIG 1

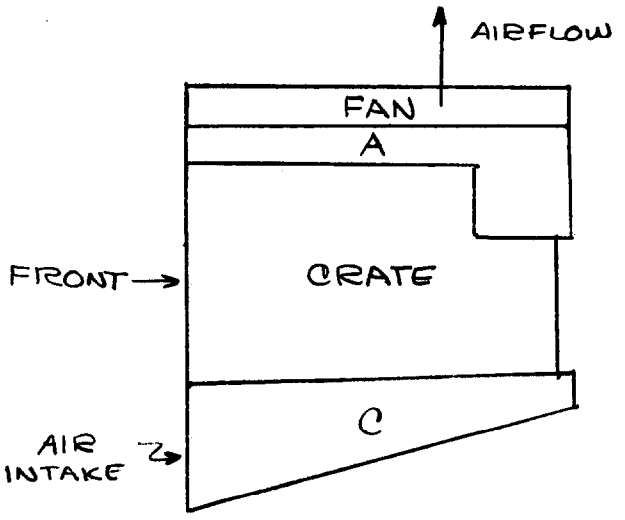
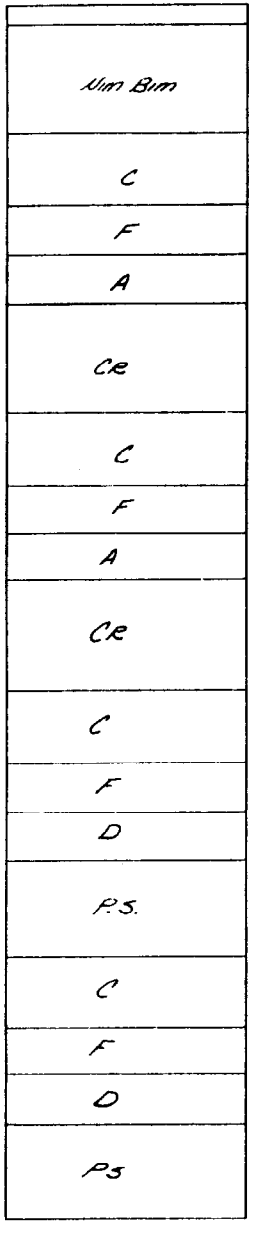

AIRFLOW
FAN
A
FRONT
CRATE
C
AIR INTAKE

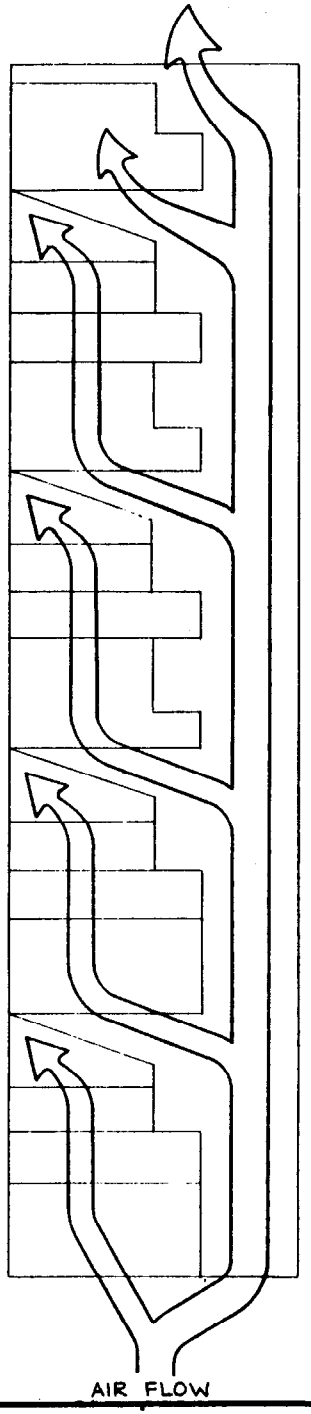
FIG 2

REVISIONS			
SYM	DESCRIPTION	DRAWN / APPD.	DATE / DATE

TM-0821



FRONT VIEW



RIGHT SIDE VIEW

ITEM NO.	PART NO.	DESCRIPTION	QTY. REQ.

PARTS LIST

UNLESS OTHERWISE SPECIFIED			ORIGINATOR	HALDEMAN 11-27-76
FRACTIONS	DECIMALS	ANGLES	DRAWN	KLINE KREBS 11-28-76
±	±	±	CHECKED	
1. BREAK ALL SHARP EDGES 1/64 MAX.			APPROVED	
2. DO NOT SCALE DWG.			APPROVED	
3. DIMENSIONING IN ACCORD WITH USASI Y14.5 STD's.			USED ON	
√ MAX. ALL MACHINED SURFACES			MATERIAL-	

NATIONAL ACCELERATOR LABORATORY
U.S. ATOMIC ENERGY COMMISSION

BEAM SYSTEMS
E516 TRIGGER PROCESSOR
RACK COOLING LAYOUT

SCALE	FILMED	DRAWING NUMBER	REV.
		0880-MC-104554	

RUNNING

ECL CAMAC CRATE

AND

ECL CRATE CAMAC POWER SUPPLY

General

The ECL CAMAC crate is a modified Standard Engineering Co. CAMAC crate. It is purchased without the standard CAMAC dataway backplane, without the standard CAMAC power connector and without the rear rails for mounting connectors.

As these crates are constructed, a Fermilab designed ECL CAMAC dataway backplane is added as well as the ECL power connector and machined rails for the ECL CAMAC I/O connectors. One rear rail is machined so that only ECL CAMAC cards that have a matching keyway can be installed in the crate.

The dataway connector is a Viking 86 pin connector soldered to the ECL CAMAC dataway backplane spaced at standard CAMAC dimensions. The power connector is a Burndy 48 pin connector to bring in -5.2 volts, -2.0 volts, +6 volts, -6 volts, and the remote sense leads for -5.2 v and -2 v to the crate.

A standard CAMAC crate controller (TTL logic levels) plugs into slots 24 and 25. Slot 23 contains Module ECL-1, TTL/ECL translator, which converts the crate controller TTL logic levels to dataway ECL logic levels for the ECL CAMAC modules in slots 1 through 22. All slots have +6 volts available so that modules such as CAMAC Branch Terminators and Branch Highway Display Modules can be installed in slots 21 and 22 in the same fashion as that of an all TTL level parallel CAMAC system.

Tables 1 and 2 show the ECL CAMAC dataway pinouts. Tables 3 and 4 show the crate power supply pin allocations. Table 5 shows the crate wiring for the translator module connector.

Power and ground connections are bussed to the slots using Copper strips. The -5.2, -2.0 and ground busses are designed for minimum voltage drop at high current loads. The busses for +6 and -6 and their respective returns are made from Lear Siegler buss strips since the load demands for these voltages are much less than that of the ECL levels.

The read/write lines (R/W1-R/W16), X, Q, Z, I, Busy, F, A, and reset lines are bussed on the ECL CAMAC dataway backplane PC board.

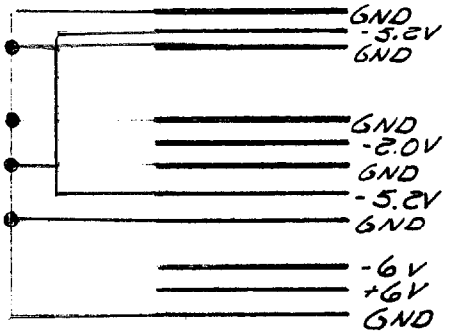
All N lines are twisted pair connected to the appropriate backplane pins.

CHECKOUT OF ECL CAMAC CRATES

The signal connections in the ECL CAMAC crate are either on the bussed PC traces on the ECL dataway backplane or made up with twisted pair wire from the control slots (23, 24, or 25) to the appropriate wire wrap pin on the Viking 86 pin connector.

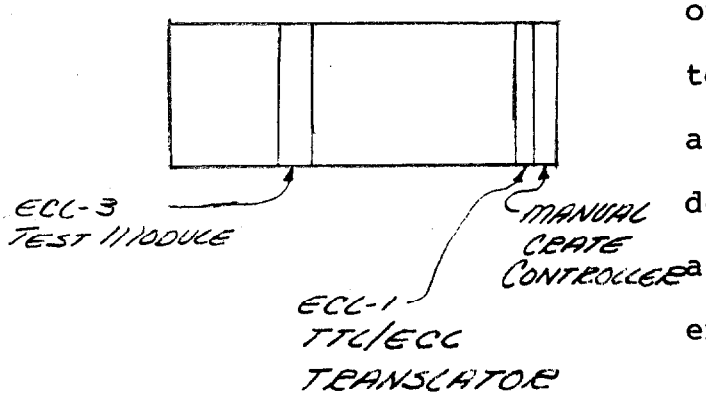
The voltage connections consist of a large cross section copper buss strip distribution pattern. In a loaded crate, the voltage drop from the center of the buss where the sense leads are connected to the end of the buss is only 15 millivolts.

The test procedure for the ECL CAMAC crate consists of testing the power distribution system and testing the logic signal connections.



As in the drawing, all ground connections are bussed together and the two -5.2 V busses are also tied together.

Using an ohmmeter, continuity tester, etc. make certain that the -5.2, -2.0, +6, -6 busses are not accidentally shorted to ground or tied to each other. The physical layout of the buss bars in the close quarters of the backplane demands that the initial checkout of the crate be very thorough to remove any construction gremlins caused by high temperature soldering of the Copper strips.



Testing the logic signals on the crate consists of checking to see that the bussed signals are present at each slot without degradation. These can be viewed at slot 1 (1) since this is the end of the buss.

The bussed signals in the crate are:

Busy	F4	A2	I
S1	F2	A1	Reset
S2	F1	X	R/W 1-16
F16	A8	Q	
F8	A4	Z	

Refer to tables for contact allocation on these bussed signals.

Testing of R/W 1-16 can be accomplished by F(16.AØ.DATA.N to the slot containing ECL-3 test module.

The N lines are individually connected to each slot from slot 23, the translator. The crate controller is set to select each slot and an oscilloscope is used to make certain that the correct N signal is present at each slot when it is addressed. This signal is present at pin 23R of a normal ECL CAMAC slot.

Reset is tested by introducing a reset input at the translator and then observing the signal along the ECL backplane buss. Since this is bussed it can be observed at N1 with the other bussed signals. Reset is allocated to pin 36R on the backplane.

Common problems located during the checkout of the existing 7 ECL CAMAC crates include:

A. Solder shorts between Copper strips in the power distribution network.

B. Solder blobs on dataway backplane caused by fallout from soldering the busses.

C. Incorrectly trimmed wires touching in wrong places.

D. Hokey connections on crimps for the connector pins on the translator preventing the signals from ever reaching the dataway backplane.

E. Lear Siegler buss bars crushed and pinched when forced down over V_{TT} terminating resistors causing a short circuit failure (±6 volt buss bars where they cross the resistors).

F. PC board problems with backplane board. Combination of artwork and etching problems. Cured with skillful application of Dremel Motor Tool Technology.

ECL CAMAC Power Supply

The ECL CAMAC power supply consists of four commercial supplies packaged in a nineteen-inch, rack-mountable case seven inches high. The voltage outputs and current capabilities are listed below.

	Maximum Output Current		
Voltage	40°C	60°C	Regulation
-5.2V	100A	65A	Switching
-2.0V	50A	35A	Switching
+6.0V	9A	7.5A	Linear
-6.0V	2.5A	2A	Linear

The power supplies are all overvoltage and overcurrent protected; the -5.2V and -2.0V supplies are remote sensed at the ECL crate backplane.

(Prepared by M. Haldeman, J. Maenpaa, 10/78)

TABLE I

CONTACT ALLOCATION FOR ECL MODULES AND ECL CAMAC CRATE

	Normal Station		Slot 23 (TTL/ECL Translator)	
	L	R	L	R
1.	GND	GND	GND	N1
2.	GND	GND	GND	N2
3.	-5.2	-5.2	-5.2	N3
4.	-5.2	-5.2	-5.2	N4
5.	GND	GND	GND	N5
6.	GND	GND	GND	N6
7.	R/W16	R/W15	R/W16	R/W15
8.	R/W14	R/W13	R/W14	R/W13
9.	R/W12	R/W11	R/W12	R/W11
10.	R/W10	R/W9	R/W10	R/W9
11.	R/W8	R/W7	R/W8	R/W7
12.	R/W6	R/W5	R/W6	R/W5
13.	R/W4	R/W3	R/W4	R/W3
14.	R/W2	R/W1	R/W2	R/W1
15.	X	Q	X	Q
16.	Z	I	Z	I
17.	Busy	F16	Busy	F16
18.	F8	F4	F8	F4
19.	F2	F1	F2	F1
20.	A8	A4	A8	A4
21.	A2	A1	A2	A1
22.	S1	S2	S1	S2
23.	Open	N	N7	N8
24.	GND	GND	GND	N9
25.	GND	GND	GND	N10
26.	-2	-2	-2	N11
27.	-2	-2	-2	N12
28.	GND	GND	GND	N13
29.	GND	GND	GND	N14
30.	-5.2	-5.2	-5.2	N15
31.	-5.2	-5.2	-5.2	N16
32.	GND	GND	GND	N17
33.	GND	GND	GND	N18
34.	Free Buss	Free Buss	N19	N20
35.	Free Buss	Free Buss	N21	N22
36.	LA	Reset	LA	Reset
37.	LB	-24	LB	-24
38.	LC	-6	LC	-6
39.	LD	Free Buss	LD	Free Buss
40.	Free Buss	Free Buss	Free Buss	Free Buss
41.	Free Buss	+24	Free Buss	+24
42.	Free Buss	+6	Free Buss	+6
43.	GND	GND	GND	GND

TABLE 2

Merle Haldeman 1/10/78
Revised 2/23/78

FUNCTION CODES

R/W	CODE F( )	FUNCTION
R	0	Read Group 1 Register
R	1	Read Group 2 Register
R	2	Read and Clear Group 1 Register
R	3	Read Complement of Group 1 Register
R	4	Non-standard
R	5	Reserved
R	6	Non-standard
R	7	Reserved
	8	Test Look-at-Me
	9	Clear Group 1 Register
	10	Clear Look-at-Me
	11	Clear Group 2 Register
	12	Non-standard
	13	Reserved
	14	Non-standard
	15	Reserved
W	16	Overwrite Group 1 Register
W	17	Overwrite Group 2 Register
W	18	Selective Set Group 1 Register
W	19	Selective Set Group 2 Register
W	20	Non-standard
W	21	Selective Clear Group 1 Register
W	22	Non-standard
W	23	Selective Clear Group 2 Register
	24	Disable
	25	Execute
	26	Enable
	27	Test Status
	28	Non-standard
	29	Reserved
	30	Non-standard
	31	Reserved

ECL CAMAC

CONTACT ALLOCATION AT A NORMAL STATION

(Viewed from front of crate)

		PIN Nos.				
	GND ECL	0	1	1R	0	GND ECL
	GND ECL	0	2	2R	0	GND ECL
	-5.2 volts	-5.2	3	3R	-5.2	-5.2 Volts
	-5.2 volts	-5.2	4	4R	-5.2	-5.2 Volts
	GND ECL	0	5	5R	0	GND ECL
	GND ECL	0	6	6R	0	GND ECL
	MSB	R/W16	7	7R	R/W15	
Read		R/W14	8	8R	R/W13	Read
Write		R/W12	9	9R	R/W11	Write
Bus		R/W10	10	10R	R/W9	Bus
Lines		R/W 8	11	11R	R/W7	Lines
		R/W 6	12	12R	R/W5	
		R/W 4	13	13R	R/W3	
		R/W 2	14	14R	R/W1	LSB
	Command Accepted	X	15	15R	Q	Response
	Initialization	Z	16	16R	I	Inhibit
	BUSY	B	17	17R	F16	Function
	FUNCTION	F8	18	18R	F4	Function
	FUNCTION	F2	19	19R	F1	Function
	SUB ADDRESS	A8	20	20R	A4	Sub Address
	SUB ADDRESS	A2	21	21R	A1	Sub Address
	STROBE 1	S1	22	22R	S2	Strobe 2
	OPEN		23	23R	N	Station Number
	GND ECL	0	24	24R	0	GND ECL
	GND ECL	0	25	25R	0	GND ECL
	-2.0 VOLTS DCC	-2	26	26R	-2.0	-2.0 Volts
	-2.0 VOLTS DC	-2	27	27R	-2.0	-2.0 Volts
	GND ECL	0	28	28R	0	GND ECL
	GND ECL	0	29	29R	0	GND ECL
	-5.2 volts	-5.2	30	30R	-5.2	-5.2 Volts
	-5.2 volts	-5.2	31	31R	-5.2	-5.2 Volts
	GND ECL	0	32	32R	0	GND ECL
	GND ECL	0	33	33R	0	GND ECL
	FREE BUS	R	34	34R		FREE BUS
	FREE BUS		35	35R		FREE BUS
	Look-at-Me	LA	36	36R	R	BUSED RESET
	Look-at-Me	LB	37	37R	-24	-24V dc (optional)
	Look-at-Me	LC	38	38R	-6	-6V dc (optional)
	Look-at-Me	LD	39	39R		FREE BUS
	FREE BUS		40	40R		FREE BUS
	FREE BUS		41	41R	+24	+24V dc (optional)
	FREE BUS		42	42R	+6	+6V dc
GND (±6 volts)		0	43	43R	0	GND (±6 volts)

GROUP 2 REGISTERS ADDRESS ASSIGNMENTS

A(12) LAM Source Register.
A(13) LAM Mask.
A(14) "Masked" LAM's.
A(15) Module Identifying Number.

TABLE 3

ECL CAMAC

FUNCTION CODES

R/W	CODE F( )	FUNCTION
R	0	Read Group 1 Register
R	1	Read Group 2 Register
R	2	Read and Clear Group 1 Register
R	3	Read Complement of Group 1 Register
R	4	Non-standard
R	5	Reserved
R	6	Non-standard
R	7	Reserved
	8	Test Look-at-Me
	9	Clear Group 1 Register
	10	Clear Look-at-Me
	11	Clear Group 2 Register
	12	Non-standard
	13	Reserved
	14	Non-standard
	15	Reserved
W	16	Overwrite Group 1 Register
W	17	Overwrite Group 2 Register
W	18	Selective Set Group 1 Register
W	19	Selective Set Group 2 Register
W	20	Non-standard
W	21	Selective Clear Group 1 Register
W	22	Non-standard
W	23	Selective Clear Group 2 Register
	24	Disable
	25	Execute
	26	Enable
	27	Test Status
	28	Non-standard
	29	Reserved
	30	Non-standard
	31	Reserved

CONTACT ALLOCATION AT STATION 23

(Viewed from front of crate)

		PIN Nos.				
GND ECL	0	1	N1			Station Number
GND ECL	0	2	N2			
-5.2 volts	-5.2	3	N3			
-5.2 volts	-5.2	4	N4			
GND ECL	0	5	N5			
GND ECL	0	6	N6			
MSB	R/W16	7	7R	R/W15		Read Write Bus Lines
Read	R/W14	8	8R	R/W13		
Write	R/W12	9	9R	R/W11		
Bus	R/W10	10	10R	R/W9		
Lines	R/W 8	11	11R	R/W7		
	R/W 6	12	12R	R/W5		
	R/W 4	13	13R	R/W3		
	R/W 2	14	14R	R/W1	LSB	
Command Accepted	X	15	15R	Q	Response	
Initialization	Z	16	16R	I	Inhibit	
BUSY	B	17	17R	F16	Function	
FUNCTION	F8	18	18R	F4	Function	
FUNCTION	F2	19	19R	F1	Function	
SUB ADDRESS	A8	20	20R	A4	Sub Address	
SUB ADDRESS	A2	21	21R	A1	Sub Address	
STROBE 1	S1	22	22R	S2	Strobe 2	
STATION NUMBER	N7	23	23R	N8		Station Number
GND ECL	0	24	24R	N9		
GND ECL	0	25	25R	N10		
-2.0 VOLTS DCC	-2	26	26R	N11		
-2.0 VOLTS DC	-2	27	27R	N12		
GND ECL	0	28	28R	N13		
GND ECL	0	29	29R	N14		
-5.2 volts	-5.2	30	30R	N15		
-5.2 volts	-5.2	31	31R	N16		
GND ECL	0	32	32R	N17		
GND ECL	0	33	33R	N18		
STATION NUMBER	N19	34	34R	N20		
STATION NUMBER	N21	35	35R	N22		
Look-at-Me	LA	36	36R	R	BUSED RESET	
Look-at-Me	LB	37	37R	-24	-24V dc (optional)	
Look-at-Me	LC	38	38R	-6	-6V dc (optional)	
Look-at-Me	LD	39	39R		FREE BUS	
FREE BUS		40	40R		FREE BUS	
FREE BUS		41	41R	+24	+24V dc (optional)	
FREE BUS		42	42R	+6	+6V dc	
GND (±6 volts)	0	43	43R	0	GND (±6 volts)	

GROUP 2 REGISTERS ADDRESS ASSIGNMENTS

A(12) LAM Source Register.
A(13) LAM Mask.
A(14) "Masked" LAM's.
A(15) Module Identifying Number.

A -5.2V	a +6V
B -5.2V	b +6V
C -5.2V	c +6V
D -5.2V	d -5.2V GND
E -5.2V	e -5.2V GND
F -2.0V	f -5.2V GND
G -2.0V	g -5.2V GND
H -2.0V	h -5.2V GND
J -2.0V	i -6V
K -2.0V	j -2.0 GND
L -5.2V GND	k -2.0 GND
M -5.2V GND	m +6V GND
N -5.2V GND	n +6V GND
P -5.2V GND	p +6V GND
R -5.2V GND	q -6V GND
S -2.0V GND	r -6V GND
T -2.0V GND	s -6V GND
U -2.0V GND	t REMOTE
V -5.2V	u REMOTE
W -5.2V	v -6V
X -5.2V	w -5.2V SENSE - SENSE
Y -5.2V	x -5.2V SENSE + SENSE
Z -5.2V	y -2.0 SENSE - SENSE
	z -2.0 SENSE + SENSE
	aa -6V

TABLE 4

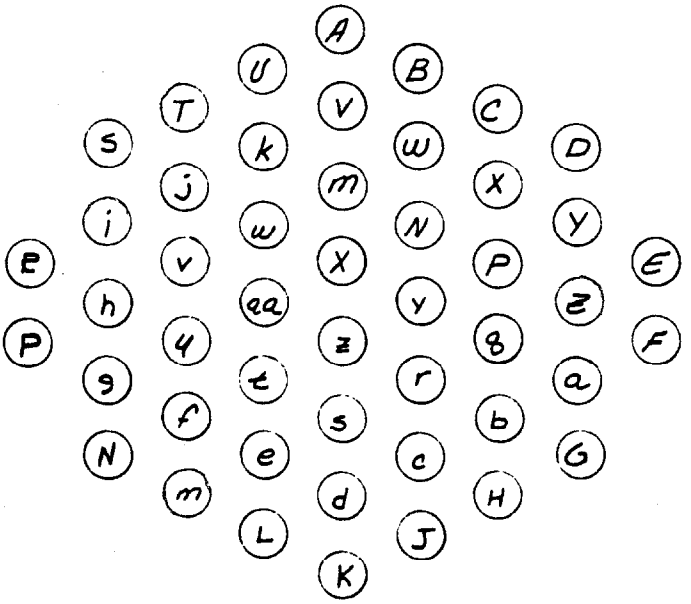
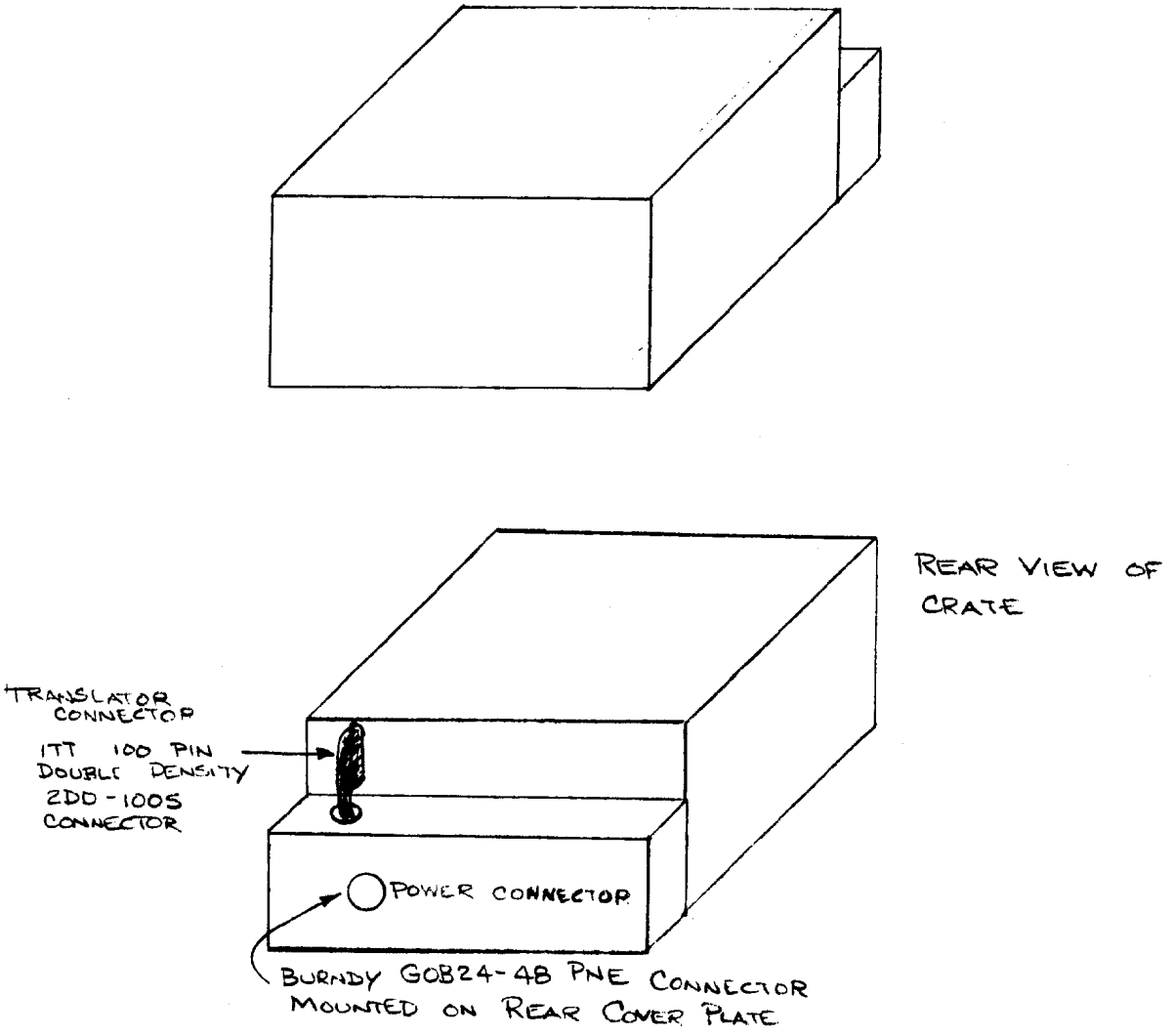


TABLE 5

BUNDY CONNECTOR
60B24-48 PNE
MOUNTED ON CBATE


REAR VIEW OF CRATE
TRANSLATOR CONNECTOR
ITT 100 PIN DOUBLE DENSITY 2DD-100S CONNECTOR
POWER CONNECTOR
BURNDY GOB24-48 PNE CONNECTOR MOUNTED ON REAR COVER PLATE

ECL MODULES

Number	Description	Designer
ECL-0	ECL Kludge	Krebs
ECL-1	TTL/ECL Translator	Barsotti/Hance
ECL-2	Memory Look-Up	Barsotti
ECL-3	ECL CAMAC Test Module	Hance
ECL-4	Memory Stack	Haldeman/Haynes
ECL-6	PWC Data Receiver and Centroid Processor	Hance
ECL-7	PWC Data Test Transmitter	Hance
ECL-8	Track Finder Do Loop Controller	Barsotti
ECL-9	Track Finder-1	Barsotti
ECL-10	Track Finder-2	Barsotti
ECL-11	Do Loop Controller/Test Transmitter	Haynes
ECL-12	Quad Scaler	Haldeman/Soszynski
ECL-13	Vertex Parameter Module	Soszynski
ECL-14	General Logic Module	Haynes
ECL-15	Fan Out Module	Soszynski
ECL-17	Output Level Converter	Haldeman
ECL-19	TDC Data Receiver	Treptow
ECL-20	Strobed ECL CAMAC Test Module	Hance

ECL Kludge Card

General Description

This general purpose kludge module is designed for research and development on ECL system modules and for in-house manufacture of low quantity ECL systems modules or ECL test modules. It is a modified Camac design and should only be used in conjunction with an ECL Camac Crate and ECL Camac Power Supply. A list of the contact allocation for ECL modules and ECL Camac crates is shown in Table I. Do not plug ECL modules into a standard Camac Crate because this pin-to-signal relationship will not match.

P.C. Card Specs

Each P.C. card (no. 0880-MC-104281) is .062" thick G10 or F4 epoxy resin fiberglass with 2 oz. copper on both sides. Holes and conductive foils are .001" ± 10% electro-deposited copper plus .001" ± 10% electro-deposited and reflowed 60/40 lead-tin alloy. Outside physical dimensions of this card are shown in the figure (Drwg. no. 0880-MC-104553).

P.C. Card Preparation

Each card may be used as is when building an Active Extender Board. Hole spacings at front allow installation of a right angle 36-pin I/O connector (Viking No. 3VH18/1JND5 or equal) and a right angle 86-pin dataway connector (Viking No. 3VH43/1JND5 or equal). However, brackets and other mounting hardware for these connectors do not exist and would, therefore, have to be designed and manufactured.

Bypass Capacitors

Bypass capacitors (-5.2 v to ECL ground; -2.0 v to ECL ground) are .01 μF, ±20% and should be of the ceramic disk variety. Due to lack of space, capacitor leads cannot be clipped if I.C. sockets are installed. Therefore, capacitors must be inserted, soldered and leads clipped before installation of any additional components.

I.C. Packages

Each card may incorporate as many as 62 16-pin packages. Eight of these I.C. locations will also accept a 24-pin package (see Figure). Each I.C. package must be used in conjunction with a wire wrap socket such as Augat nos: 516-AG10F-2 (16-pin) and 524-AG10F-2 (24-pin).

Power

Power is supplied thru the dataway insertion connector via one -2.0 volt bus and two -5.2 volt busses. Each -5.2 volt bus powers 50% of the I.C. locations at pin 8 of the 16-pin packages and pin 12 of the 24-pin packages. Each bus must be cut at I.C. locations that need a different power pin arrangement. These two busses may be jumpered together at each of 13 locations. Each bus must be bypassed to ECL ground (near insertion connector) with a 100 pF, ±5% silver-mica capacitor and a 45 μF tantalum capacitor. An ICTE-5 transient suppressor provides over-voltage protection. Power busses are located on wire-wrap (non-component) side of P.C. card.

+6 v and -6 v are available at the insertion connector thru

pin nos. 42R and 38R respectively. A ± 24V power supply must be added if these voltages are needed.

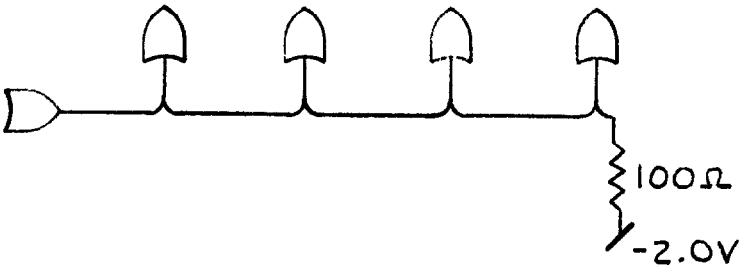
Ground

ECL ground (located on component side) is supplied thru the dataway insertion connector and grounds all IC.'s at pins 1 and 16 (16-pin packages) or pins 1 and 24 (24-pin packages). This ground must be cut at I.C. locations that need a different ground pin arrangement. Crate ground (from ±6 v power supply) is supplied thru the insertion connector at pins 43R and 43L. It is isolated from ECL ground but the two grounds may be jumpered together at any of twelve places.

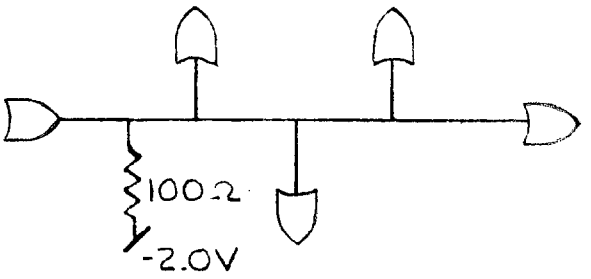
Signal Terminations and Wiring Guidelines

All signals must be terminated at the receiving end with either 100Ω, 1/8 watt carbon resistors to -2.0 volts or 510Ω, 1/8 watt carbon resistors to -5.2 volts as indicated on the design schematic. When several receivers (inputs) are connected to one output, the wiring must daisy-chain the receivers (no tree structure allowed) with the terminating resistor wired just after the last receiver in the chain as shown below.

Must be wired like this.



Must not be wired like this.



Additional assembly techniques are listed below:

1) Use twisted pair on all inputs and outputs to front panel.
2) Keep drivers and receivers close to front panel.
3) When using front panel mounting ribbon cable connectors, do not use wire wrap posts for an interconnector. Go directly to the I.C. with the other end of the cable. This means separation and stripping the leads.
4) Do not cross lines when bringing (F and A) or (R-W) signals on board, i.e. keep F and A signal separate from R-W signals and also their I.C.'s.
5) Do not bundle wires when making on-board interconnections. Use many different paths.
6) Long parallel runs should be avoided - use separate routes.

Rails

Rails must be of the Standard Camac type as supplied by Nuclear Specialities Incorporated or Standard Engineering Corporation.

Front Panels

Standard double-width Camac front panels may be used with the exception of multiple card applications.

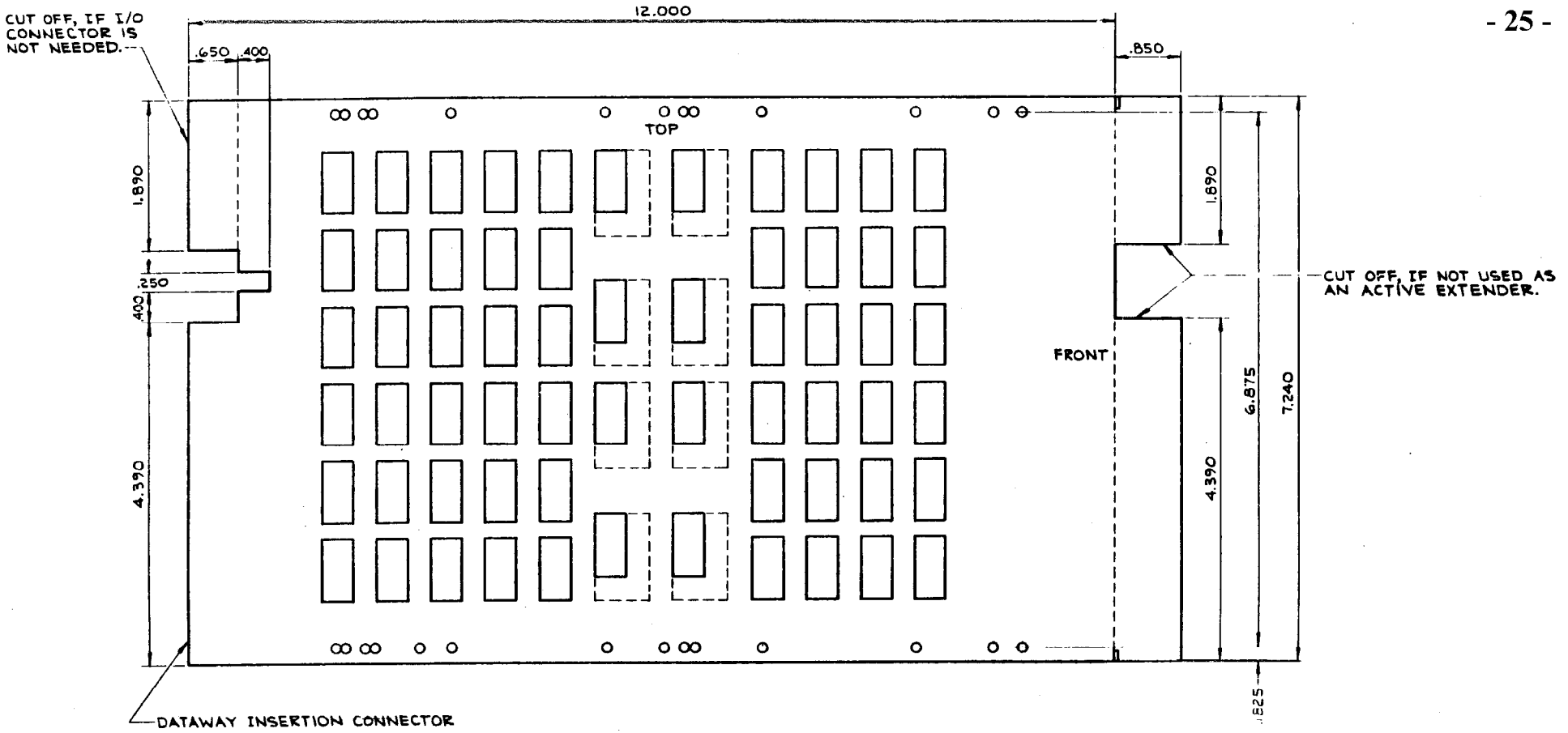
(Prepared by J. Krebs, 11/78)

TABLE I

CONTACT ALLOCATION FOR ECL MODULES AND ECL CAMAC CRATE

	Normal Station		Slot 23 (TTL/ECL Translator)	
	L	R	L	R
1.	GND	GND	GND	N1
2.	GND	GND	GND	N2
3.	-5.2	-5.2	-5.2	N3
4.	-5.2	-5.2	-5.2	N4
5.	GND	GND	GND	N5
6.	GND	GND	GND	N6
7.	R/W16	R/W15	R/W16	R/W15
8.	R/W14	R/W13	R/W14	R/W13
9.	R/W12	R/W11	R/W12	R/W11
10.	R/W10	R/W9	R/W10	R/W9
11.	R/W8	R/W7	R/W8	R/W7
12.	R/W6	R/W5	R/W6	R/W5
13.	R/W4	R/W3	R/W4	R/W3
14.	R/W2	R/W1	R/W2	R/W1
15.	X	Q	X	Q
16.	Z	I	Z	I
17.	Busy	F16	Busy	F16
18.	F8	F4	F8	F4
19.	F2	F1	F2	F1
20.	A8	A4	A8	A4
21.	A2	A1	A2	A1
22.	S1	S2	S1	S2
23.	Open	N	N7	N8
24.	GND	GND	GND	N9
25.	GND	GND	GND	N10
26.	-2	-2	-2	N11
27.	-2	-2	-2	N12
28.	GND	GND	GND	N13
29.	GND	GND	GND	N14
30.	-5.2	-5.2	-5.2	N15
31.	-5.2	-5.2	-5.2	N16
32.	GND	GND	GND	N17
33.	GND	GND	GND	N18
34.	Free Buss	Free Buss	N19	N20
35.	Free Buss	Free Buss	N21	N22
36.	LA	Reset	LA	Reset
37.	LB	-24	LB	-24
38.	LC	-6	LC	-6
39.	LD	Free Buss	LD	Free Buss
40.	Free Buss	Free Buss	Free Buss	Free Buss
41.	Free Buss	+24	Free Buss	+24
42.	Free Buss	+6	Free Buss	+6
43.	GND	GND	GND	GND

REVISIONS			
SYM	DESCRIPTION	DRAWN / APPD.	DATE



ITEM NO.	PART NO.	DESCRIPTION	QTY. REQ.

PARTS LIST

UNLESS OTHERWISE SPECIFIED			ORIGINATOR	H. JAMES KREBS	11-17-78
FRACTIONS	DECIMALS	ANGLES	DRAWN		
±	±.005	±	CHECKED		
1. BREAK ALL SHARP EDGES 1/64 MAX.			APPROVED		
2. DO NOT SCALE DWG.			APPROVED		
3. DIMENSIONING IN ACCORD WITH USASI Y14.5 STD's.			USED ON		
√ MAX. ALL MACHINED SURFACES			MATERIAL-		

NATIONAL ACCELERATOR LABORATORY
U.S. ATOMIC ENERGY COMMISSION

BEAM SYSTEMS
ECL KLUDGE CARD
PHYSICAL DIMENSIONS

SCALE	FILMED	DRAWING NUMBER	REV.
FULL		0880-MC-104553	

SUBJECT: DOCUMENTATION OF: ECL-0

NAME: H. James Krebs

DATE: 11-29-78 | REVISION DATE:

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	SEE BELOW
FRONT PANEL MACHING DRAWING	
FRONT PANEL ASSEMBLY	
FRONT PANEL ARTWORK	
MODULE FINAL ASSEMBLY	
P.C. CARD COMPONENT ASSEMBLY	
P.C. CARD DRILL DRAWING	0880-MC-104281
P.C. CARD PARTS LIST	
P.C. CARD MASTER ARTWORK	0880-MD-104280
BOARD OUTLINE	0880-MC-104553
PHOTO REDUCTIONS	FP-28
SINGLE WIDTH	0880-MB-104430
DOUBLE WIDTH	0880-MB-104431

ECL/CAMAC MODULE ECL-1

- ECL Translator -
(General Purpose Module - PC Board - Single Width)

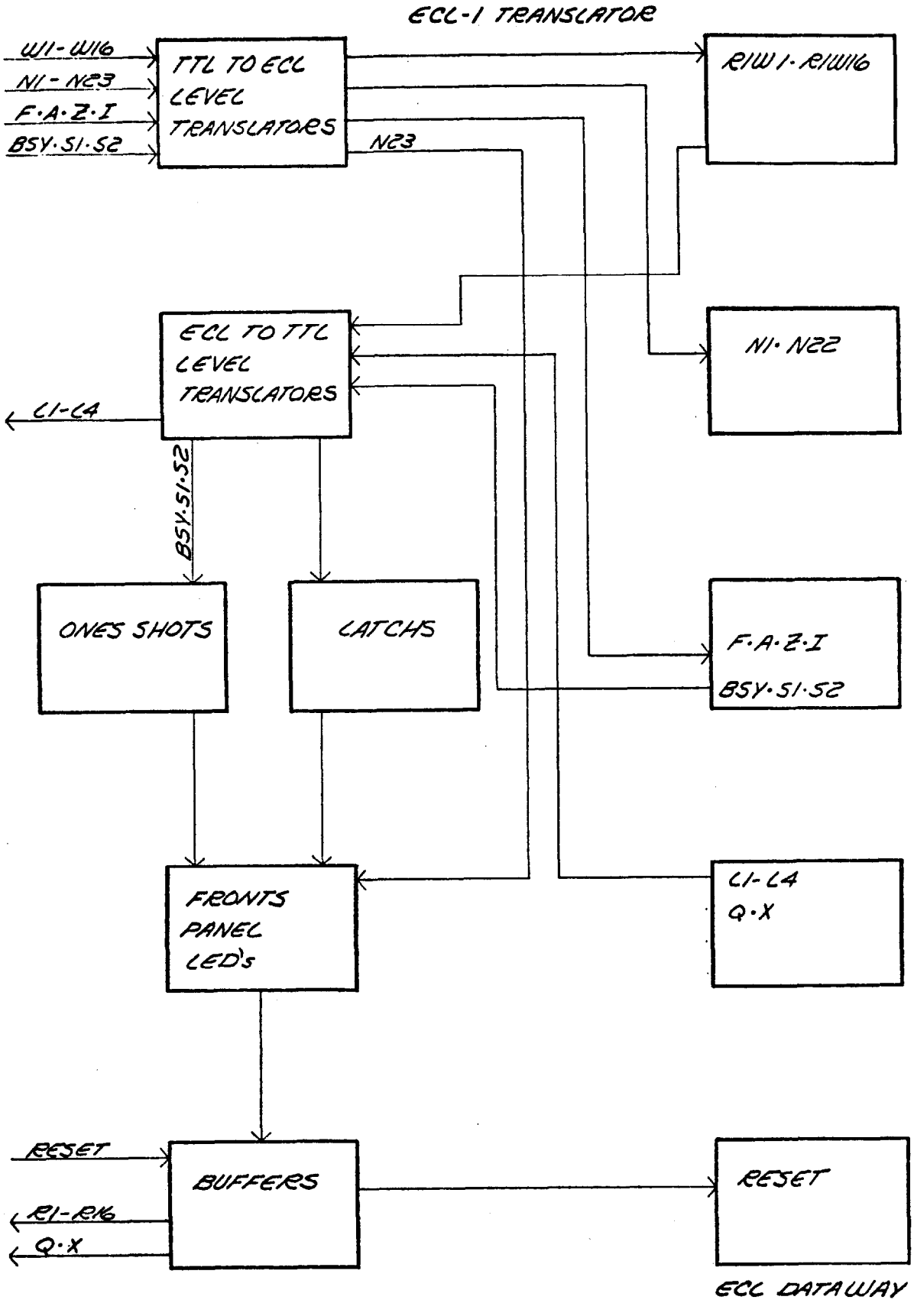
General Description

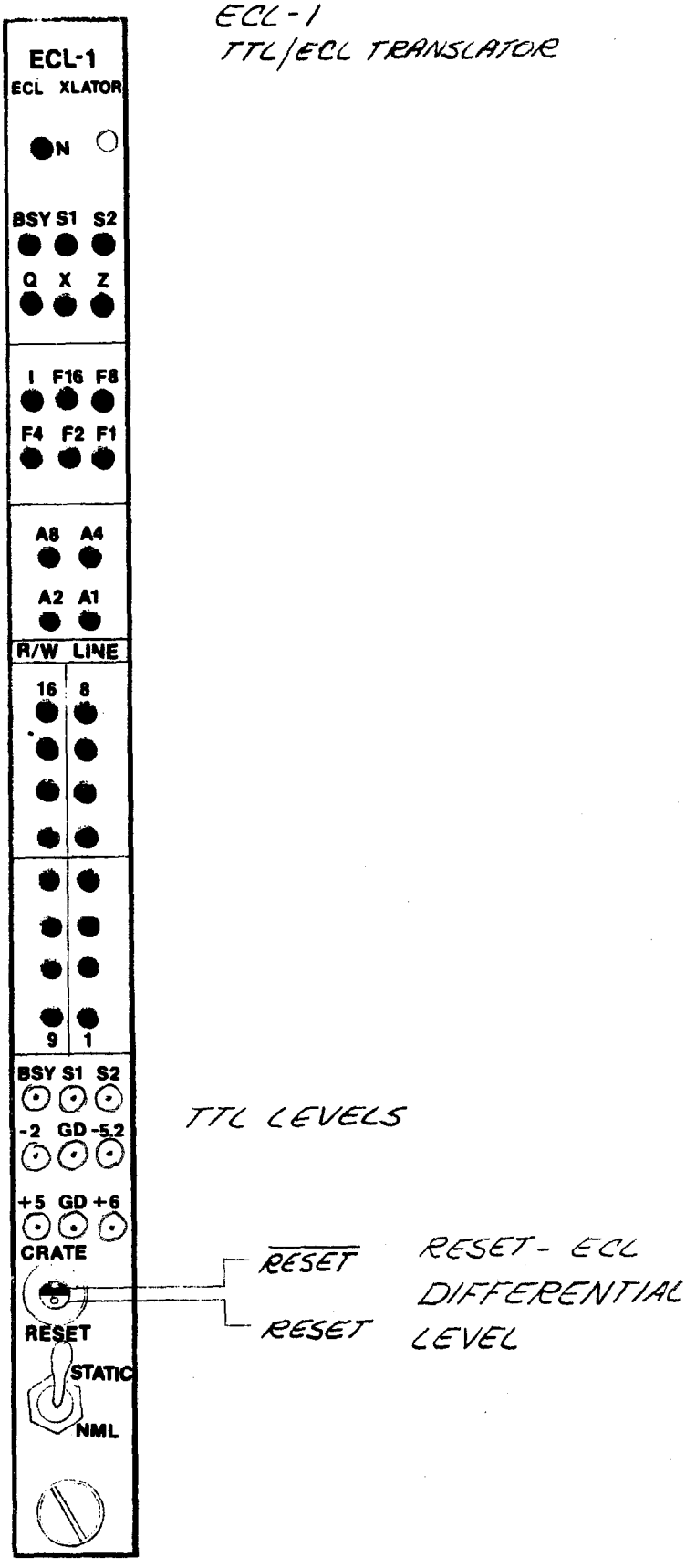
This single width module resides in slot 23 of an ECL/CAMAC crate. This module accepts conventional TTL CAMAC lines from slots 24 and 25 via a 100 pin Cannon high density connector. Translates them to ECL levels and puts them on the backplane for slots 1 - 22. To the rest of the CAMAC system the modules in slots 1 - 22 appear normal following regular CAMAC rules except that only 16 R/W lines are used.

The front panel contains CAMAC line monitoring lights, test points for voltages and timing signals, and a reset input which is buffered and put on the backplane to slots 1 - 22. The front panel contains a display mode switch, in the NORMAL position information on the display is latched and in the STATIC position the display shows the static state of the dataway.

When addressed through CAMAC this module returns Q and X for all N23 commands and can be written to and read back from using any CAMAC Write or Read command provided the display mode switch is in the NORMAL position.

(Prepared by K. Treptow - 8/30/78)


ECL-1 TRANSLATOR
W1-W16
N1-N23
F·A·Z·I
BSY·S1·S2
TTL TO ECL LEVEL TRANSLATORS
N23
R1W1-R1W16
ECL TO TTL LEVEL TRANSLATORS
N1-N22
C1-C4
BSY·S1·S2
ONES SHOTS
LATCHS
F·A·Z·I
BSY·S1·S2
FRONTS PANEL LED's
C1-C4
Q·X
RESET
BUFFERS
R1-R16
Q·X
RESET
ECL DATAWAY


ECL-1
ECL XLATOR
ON
BSY S1 S2
Q X Z
I F16 F8
F4 F2 F1
A8 A4
A2 A1
R/W LINE
16 8
9 1
BSY S1 S2
-2 GD -5.2
+5 GD +6
CRATE
RESET
STATIC
NML
ECL-1
TTL/ECL TRANSLATOR
TTL LEVELS
RESET
RESET
RESET - ECL
DIFFERENTIAL
LEVEL

FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL - CATEGORY	PAGE
BEST	EXP. 516	TM-0821	30

SUBJECT

DOCUMENTATION OF: ECL-1

NAME: H. James Krebs

DATE: 6-21-78

REVISION DATE:

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-ED-104300
FRONT PANEL MACHING DRAWING	0880-MC-104289
FRONT PANEL ASSEMBLY	0880-MC-104312
FRONT PANEL ARTWORK	0880-MC-104307
MODULE FINAL ASSEMBLY	0880-MD-104308
P.C. CARD COMPONENT ASSEMBLY	0880-MD-104310
P.C. CARD DRILL DRAWING	0880-MD-104311
P.C. CARD PARTS LIST	0880-MA-104309
P.C. CARD MASTER ARTWORK	0880-MD-104325
BOARD OUTLINE	0880-MC-104304
PHOTO REDUCTIONS	FP-29
100 PIN CONNECTOR BRACKET (TOP)	0880-MB-104287
100 PIN CONNECTOR BRACKET (BOTTOM)	0880-MB-104286
TOP RAIL MODIFICATION	0880-MB-104290

ECL/CAMAC MEMORY LOOK UP MODULE (MLU) ECL-2

General Purpose Module-Multilayer PC Board-Double Width

This is a table look up function module. The output (which may be up to 16 bits and represent several, ($\leq$ 16, variables) is a function of the input (up to 16 bit variables). The function, the table stored in a RAM, may be changed via CAMAC.

Application Examples:

Rapid function calculation
Time or pulse height calibration
High speed arithmetic
6 bit ALU: - + ÷ x cos, sin etc.
Process control and programming
Single module replacement of
  experimental fast logic
Etc.

Inputs	bits
ID (Input data)	$\leq$ 16
IR1 (Input Ready) 1	1
IR2 (Input Ready) 2	1
IR3 (Input Ready) 3	1
IR4 (Input Ready) 4	1

Outputs	bits
BID (Buffered Input Data)	16
BIR1 (Buffered Input Ready 1)	1
BIR2 (Buffered Input Ready 2)	1
BIR3 (Buffered Input Ready 3)	1
BIR4 (Buffered Input Ready 4)	1
OD (Output Data)	$\leq$ 16
OR1 (Output Ready 1)	1
OR2 (Output Ready 2)	1
OR3 (Output Ready 3)	1
OR4 (Output Ready 4)	1
OD0 } Lemo outputs of 2 LSBs	1
OD1 }	1

Note; Various bits of ID/OD may come from/go to different modules. Each IR_i/OR_i connects to one of these modules.

Operation Modes

The module may be loaded with up to 16 RAMS which may be (depending on jumper wires on the PC board) either 1024 x 1 (ECL 10415) or 4096 x 1 (ECL 10470). Most applications not desperate for speed use 4096 RAMS. Depending on the setting of a front panel ("Output Configuration") switch the data may be read out 1, 2, 4, 8 or 16 bits at a time:

Output Configuration Switch	Input Bits - 4096 (1024) RAMS	Number of Addresses	Output Bits
16	12 (10)	4096 (1024)	16
8	13 (11)	8192 (2048)	8
4	14 (12)	16384 (4096)	4
2	15 (13)	32768 (8192)	2
1	16 (14)	65536 (16384)	1

Although front panel accessing can be configured different ways, CAMAC writing and reading is always sixteen bits at a time. Appropriate software routines are necessary to properly set up the memory for the readout configuration used (see below).

The MLU is accessed statically by presenting an address to the ribbon cable connector (input data) and a ready to each two-pin lemo connector (input ready) on the front panel. Each unused address line is interpreted as a zero, and each unused input ready line is interpreted as true. When all input readys

become true, an access delay will occur followed by all output readys going true. The access delays are typically 40 ns for modules loaded with 1024 bit RAMS and 55 ns for modules loaded with 4096 bit RAMS. When the ORs come on, the OD is meaningful. If OR is not on, the OD may be changing in a meaningless manner. The last IR must arrive after the arrival of the last ID variable. An on board timing resistor selects the basic delay time for each type RAM. This resistor must be selected and loaded when the module is assembled (refer to the schematic). In addition, the delay time between all input readys going true and all output readys going true can be adjusted over a range of approximately 15 ns by a front panel potentiometer. This is to allow for optimizing each individual MLU for speed since there is a significant variation in the speed of individual ECL RAMs. Removing any input ready will remove all output readys but output data will remain valid until an input address is changed.

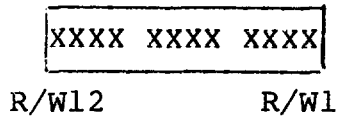
Memory Loading and Testing

The next few pages provide detailed information on memory configuration and CAMAC instructions which are necessary for writing host computer software as well as for module debugging. A pedestrian user can ignore these pages and refer to the section on software which describes a PDP-11 package that allows programming and loading of MLUs without knowledge of the details.

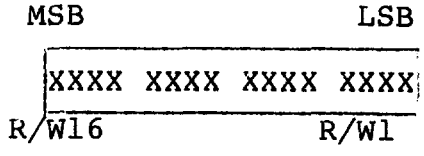
Function Codes

Q and X are returned for all valid codes.

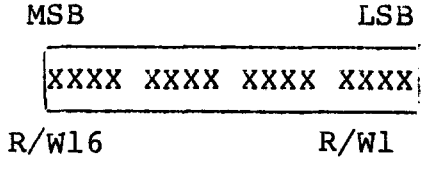
F17 A0 write CAMAC address



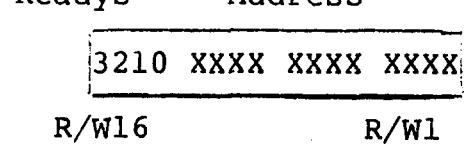
F16 AX write RAM at CAMAC address and increment CAMAC address



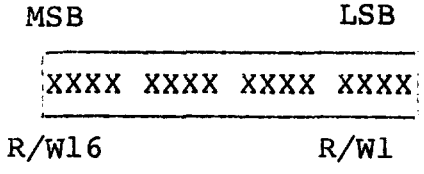
F0 AX read RAM at CAMAC address and increment CAMAC address



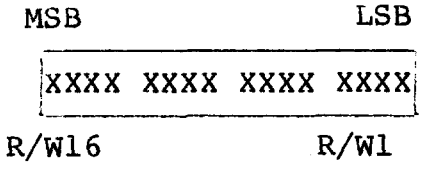
F1 A0 read CAMAC address and input readys



F2 A0 read front panel input address



F3 A0 read RAM at front panel input address



Configuration and Use

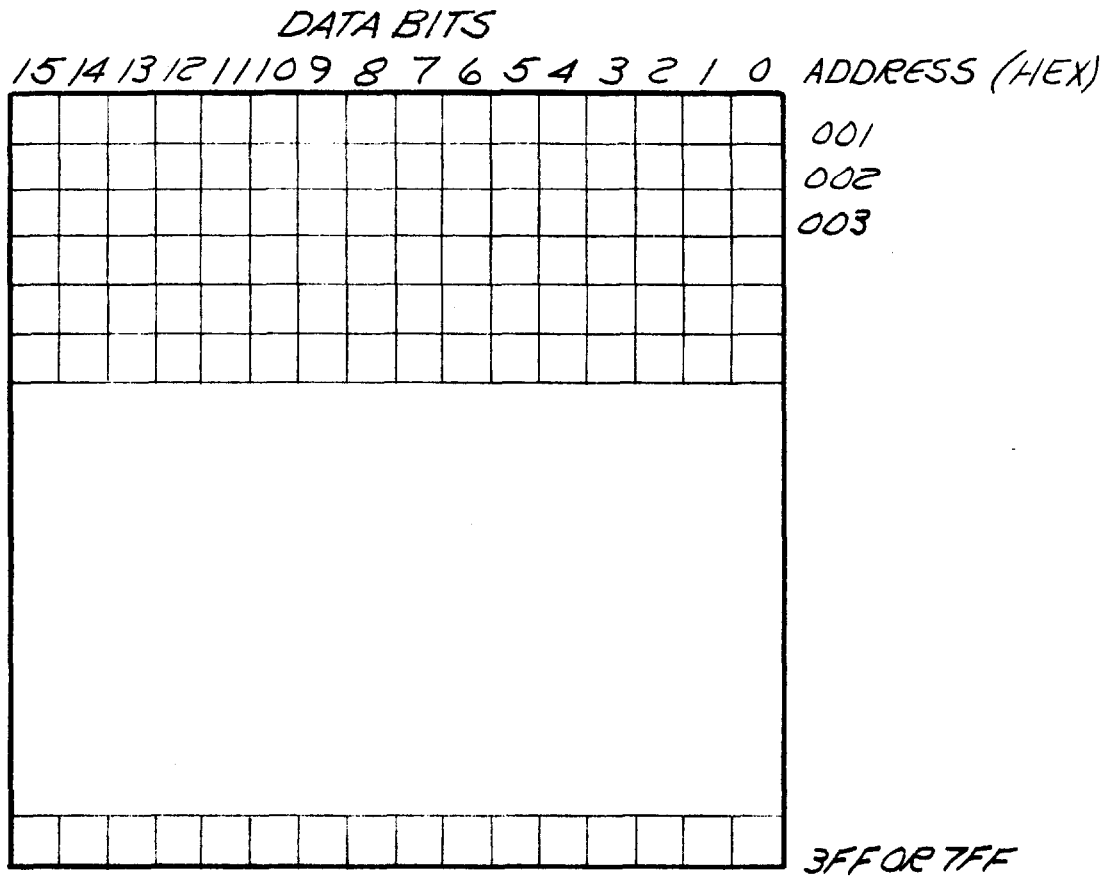
Loading of the MLU by CAMAC must be done with regard to how the data will be read out, which depends on the output configuration switch and the memory select bits of the input address.

The memory section of the MLU is composed of 16 individual random access memories (RAMs) of 1024 or 4096 bits. For CAMAC write or read operations, these circuits are handled as a 16-bit wide memory with a common address. However, when accessing is via a front panel ECL address, configuration of the memories is a function of the output configuration switch, and the front panel input address bits.

The following illustrations show how the memory is written and read via CAMAC, and read via the front panel address inputs.

CAMAC Loading

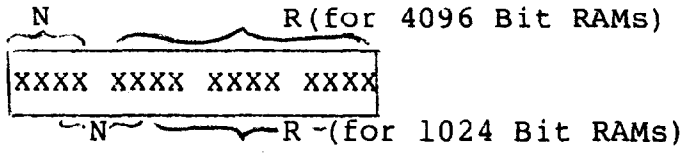
Memory is treated as 1024 or 4096 by 16. Data bits 0-15 correspond to CAMAC bits 1-16.



Front Panel Addressing

The front panel ECL input address is comprised of 16 bits, of which normally the upper 4 bits are used internally as a nibble address (N) which selects RAMs for output and steers output data to the proper bits. The remaining 12 bits are used as addresses (R) to the RAMs. If 1024 bit RAMs are used, only the 10 LSBs

are used to specify R. Also, for 1024 bit RAMs, on board jumpers can be used to select bits 13, 12, 11 and 10 as the nibble address if it is not desireable to use the upper bits. The figure below shows how the ECL input address word is broken into N, R:



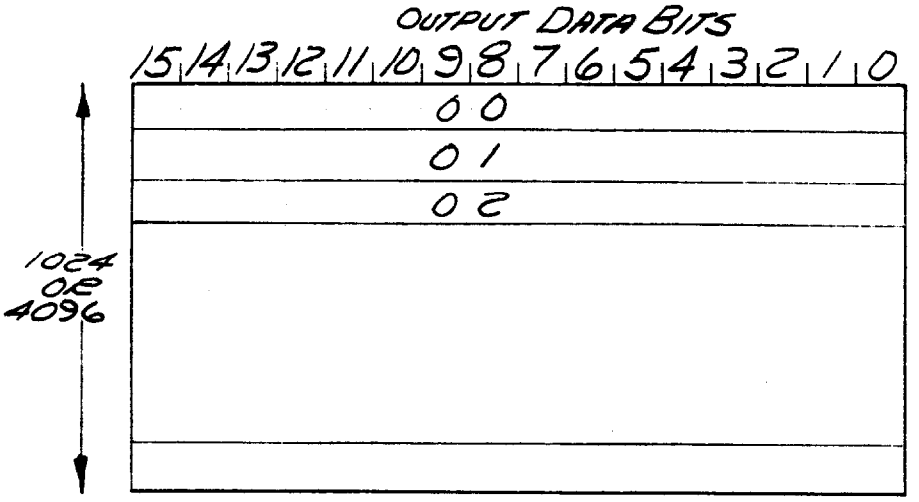
(for 1024 bit RAMs only if desired and jumpers are changed)

The following illustrations show, for each output configuration setting, the N, R addresses to the memory array: As an example of the notation used in these illustrations, (5,1) corresponds to

A15			A0
0101	0000	0000	0001

Prepared by R. Hance and T. Nash (10/26/78)

16 BIT READBACK MODE (X16)
THE OUTPUT WORD IS 16 BITS WIDE.
MEMORY ADDRESS DESIGNATED
BY N, E.



8 BIT READ BACK MODE (x8)

THE OUTPUT WORD IS 8 BITS WIDE. MEMORY ADDRESS IS DESIGNATED BY N, R.

1024 OR 4096

OUTPUT DATA BITS

7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
1, 0	0, 0
1, 1	0, 1
1, 2	0, 2

---

4 BIT READ BACK MODE (x4)

THE OUTPUT WORD IS 4 BITS WIDE. MEMORY ADDRESS IS DESIGNATED BY N, R.

1024 OR 4096

OUTPUT DATA BITS

3 2 1 0	3 2 1 0	3 2 1 0	3 2 1 0
3 0	2 0	1 0	0 0
3 1	2 1	1 1	0 1
3 2	2 2	1 2	0 2

2 BIT READBACK MODE (x2)

THE OUTPUT WORD IS 2 BITS WIDE. MEMORY ADDRESS IS DESIGNATED BY U, R

OUTPUT DATA BITS

1,0	1,0	1,0	1,0	1,0	1,0	1,0	1,0
7,0	6,0	5,0	4,0	3,0	2,0	1,0	0,0
7,1	6,1	5,1	4,1	3,1	2,1	1,1	0,1
7,2	6,2	5,2	4,2	3,2	2,2	1,2	0,2

1024 OR 4096

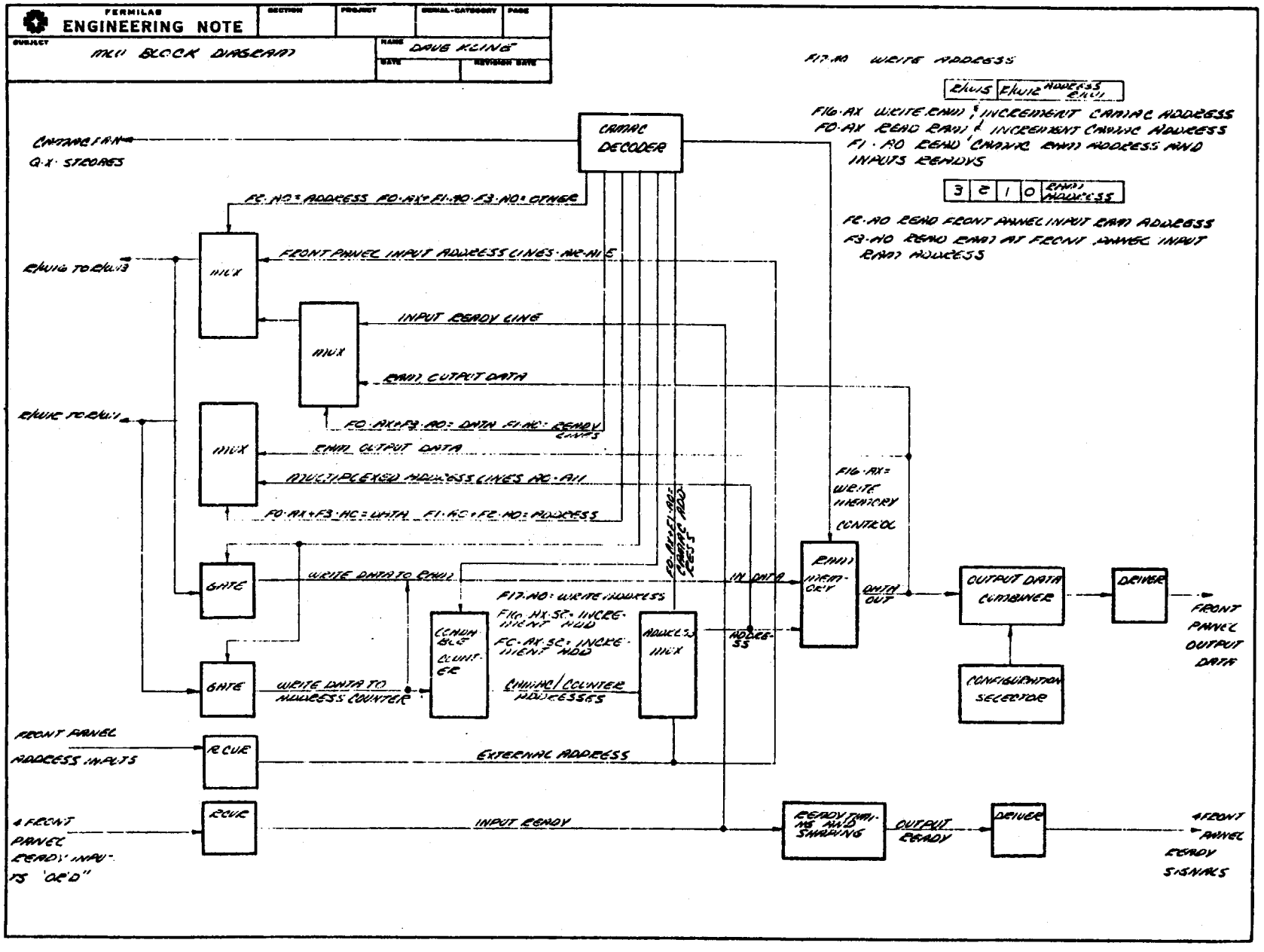
OUTPUT DATA BITS

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15,0	14,0	13,0	12,0	11,0	10,0	9,0	8,0	7,0	6,0	5,0	4,0	3,0	2,0	1,0	0,0
15,1	14,1	13,1	12,1	11,1	10,1	9,1	8,1	7,1	6,1	5,1	4,1	3,1	2,1	1,1	0,1
15,2	14,2	13,2	12,2	11,2	10,2	9,2	8,2	7,2	6,2	5,2	4,2	3,2	2,2	1,2	0,2

1024 OR 4096

1 BIT READBACK MODE (x1)

THE OUTPUT IS 1 BIT WIDE. MEMORY ADDRESS IS DESIGNATED BY U, R


FERMILAB
ENGINEERING NOTE
SUBJECT
MKII BLOCK DIAGRAM
NAME
DAVE KLINE
DATE
REVISION DATE
CRATE DECODER
CONTAINS FAN-IN & O.R. STORES
F2·NO = ADDRESS F0·AX·F1·NO·F3·NO = OTHER
MUX
FRONT PANNEL INPUT ADDRESS LINES AR-AL
EMUX TO EMU3
MUX
INPUT READY LINE
MUX
EMU1 OUTPUT DATA
EMUX TO EMU1
MUX
F0·AX·F3·AC: DATA F1·AC: READY LINES
EMUX OUTPUT DATA
MULTIPLEXED ADDRESS LINES AC-A11
F0·AX·F3·AC = DATA F1·AC·F2·NO = ADDRESS
GATE
WRITE DATA TO EMU1
GATE
WRITE DATA TO ADDRESS COUNTER
EMUX BLOCK COUNTER
F17.NO: WRITE ADDRESS
F10.AX.SC: INCREMENT MOD
F0.AX.SC: INCREMENT MOD
EMUX/COUNTER ADDRESSES
ADDRESS MUX
ADDRESS
EMU1 MEMORY
IN DATA
DATA OUT
F16·AX = WRITE MEMORY CONTROL
OUTPUT DATA COMBINER
DRIVER
FRONT PANEL OUTPUT DATA
CONFIGURATION SELECTOR
FRONT PANEL ADDRESS INPUTS
RCVR
EXTERNAL ADDRESS
4 FRONT PANEL READY INPUTS "OR'D"
2CVR
INPUT READY
READY TIMING AND STRETCHING
OUTPUT READY
DRIVER
4 FRONT PANEL READY SIGNALS
F17.NO WRITE ADDRESS
EMUS EMU2 ADDRESS EMU1
F16·AX WRITE EMU1 INCREMENT CAMAC ADDRESS
F0·AX READ EMU1 INCREMENT CAMAC ADDRESS
F1·NO READ CAMAC EMU1 ADDRESS AND INPUTS READYS
3 2 1 0 EMU1 ADDRESS
F2·NO READ FRONT PANNEL INPUT EMU ADDRESS
F3·NO READ EMU AT FRONT PANNEL INPUT EMU ADDRESS

IC 20 MAIN BOARD

$A_4A_3A_2A_1A_0$	$Q_7Q_6Q_5Q_4Q_3Q_2Q_1Q_0$
0 0 0 0 0	1 1 1 1 1 1 1 1
0 0 0 0 1	1 1 1 1 1 1 1 1
0 0 0 1 0	1 1 1 1 1 1 1 1
0 0 0 1 1	1 1 1 1 1 1 1 1
0 0 1 0 0	0 0 0 0 0 0 0 0
0 0 1 0 1	1 1 1 1 1 1 1 1
0 0 1 1 0	1 1 1 1 1 1 1 1
0 0 1 1 1	1 1 1 1 1 1 1 1
0 1 0 0 0	1 1 1 1 1 1 1 1
0 1 0 0 1	1 1 1 1 1 1 1 1
0 1 0 1 0	1 1 1 1 1 1 1 1
0 1 0 1 1	1 1 1 1 1 1 1 1
0 1 1 0 0	1 1 1 1 1 1 0 0
0 1 1 0 1	1 1 1 1 0 0 1 1
0 1 1 1 0	1 1 0 0 1 1 1 1
0 1 1 1 1	0 0 1 1 1 1 1 1
1 0 0 0 0	1 1 1 0 1 1 1 1
1 0 0 0 1	1 1 0 1 1 1 1 1
1 0 0 1 0	1 0 1 1 1 1 1 1
1 0 0 1 1	0 1 1 1 1 1 1 1
1 0 1 0 0	1 1 1 1 1 1 1 0
1 0 1 0 1	1 1 1 1 1 1 0 1
1 0 1 1 0	1 1 1 1 1 0 1 1
1 0 1 1 1	1 1 1 1 0 1 1 1
1 0 0 0 0	1 1 1 1 1 1 1 1
1 1 0 0 1	1 1 1 1 1 1 1 1
1 1 0 1 0	1 1 1 1 1 1 1 1
1 1 0 1 1	1 1 1 1 1 1 1 1
1 1 1 0 0	1 1 1 1 0 0 0 0
1 1 1 0 1	0 0 0 0 1 1 1 1
1 1 1 1 0	1 1 1 1 1 1 1 1
1 1 1 1 1	1 1 1 1 1 1 1 1

10139 Programming Chart

$\overline{RAM0}$ through $\overline{RAM\ 7}$ PROM

$Q_i = \overline{RAM_i}$ $\quad i = 0, 1, \ldots, 7$

A_o = A12 (A10)

A_1 = A13 (A11)

$\overline{A_2} = \overline{A14(A12) + A15(A13)}$

A_3 = X2 + X4

$A_4 = \overline{A15(A13) + X2 + X8}$

$\overline{CS}$ = X16+16X+170+0X+10+20+30

IC-12 PIGGYBACK BOARD

A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	1	1	1
0	0	0	1	0	0	0	0	1	1	1	1	1
0	0	0	1	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	1	1	1	1	1	0
0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	0
0	1	0	0	0	1	1	1	1	0	1	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	1	1	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0
1	1	0	1	1	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0

10139 PROGRAMMING CHART

X1,X2,X4,X8,X16 PROM

Q_0 = X1+X2

Q_1 = X1+X2+X4

Q_2 = X1+X2+X4+X8

Q_3 = X2+X4

Q_4 = X2+X4+X8

Q_5 = X4+X8

Q_6 = X4+X8+X16

Q_7 = X8+X16

A_0 = X1

A_1 = X2

A_2 = X4

A_3 = X8

A_4 = X16

$\overline{CS}$ = 0

IC-22 MAIN BOARD

A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	1	1	1	1
0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	0	1	1	1	1	1	1	0	0
0	1	0	0	1	1	1	1	1	0	0	1	1
0	1	0	1	0	1	1	0	0	1	1	1	1
0	1	0	1	1	0	0	1	1	1	1	1	1
0	1	1	0	0	1	1	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	1	1	1
0	1	1	1	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1	1	1	1
1	0	1	0	0	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1
1	0	1	1	0	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	0	0	0	0
1	1	1	1	1	0	0	0	0	1	1	1	1

10139 PROGRAMMING CHART

$\overline{\text{RAM 8}}$ THROUGH $\overline{\text{RAM 15}}$ PROM

Q_i = P/O $\overline{RAM}_i$ i = 8, 9, ..., 15

A_o = A12(A10)

A_1 = A13(A11)

$A_2 = \overline{A14(A12)+A15(A13)}$

A_3 = X2+X4

$A_4 = \overline{A15(A13)+X2+X8}$

$\overline{CS}$ = X16+16X+170+0X+10+20+30

IC-40 MAIN BOARD

A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	1	1	0	0	1	0	0	1
0	0	0	0	1	1	1	0	1	1	1	0	0
0	0	0	1	0	1	0	0	0	0	0	1	0
0	0	0	1	1	0	0	0	0	0	0	0	0
0	0	1	0	0	1	1	0	0	0	0	1	1
0	0	1	0	1	1	0	1	0	0	1	0	0
0	0	1	1	0	1	0	0	0	0	0	0	1
0	0	1	1	1	0	0	0	0	0	0	0	0
0	1	0	0	0	1	1	0	0	1	0	0	1
0	1	0	0	1	1	1	0	1	1	1	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0
1	1	0	1	1	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0

10139 PROGRAMMING CHART

CAMAC DECODING PROM

Q_0 = 0X+10+30

Q_1 = 10+20

Q_2 = 16X+170

Q_3 = 0X+16X

Q_4 = 16X

Q_5 = 170

Q_6 = 0X+10+16X

Q_7 = 16X+170+0X+10+20+30

A_0 = F16

A_1 = F2

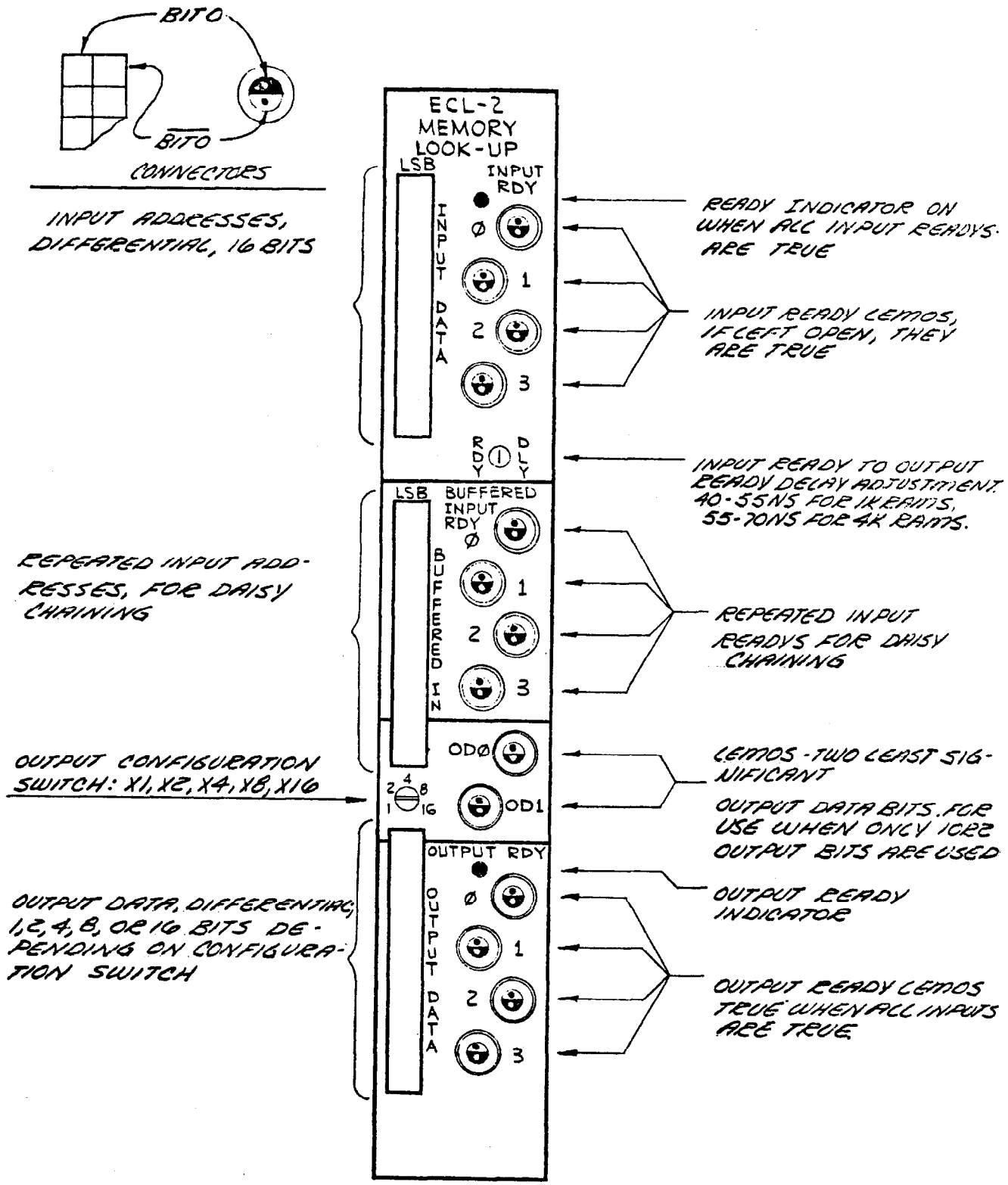
A_2 = F1

A_3 = A_8+A_4+A_2+A_1

A_4 = F_8+F_4

$\overline{CS}$ = $\overline{N}$

FRONT PANEL LAYOUT



FERMILAB

ENGINEERING NOTE

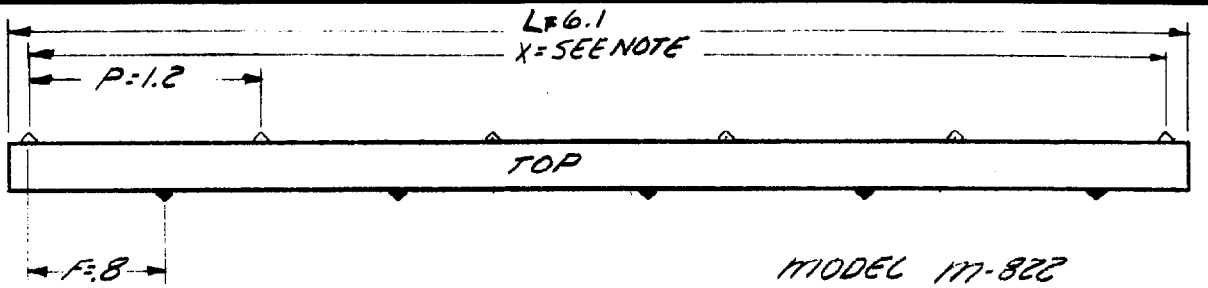
SECTION	PROJECT	SERIAL-CATEGORY	PAGE
	E-516	TM-0821	48

SUBJECT: ECL-2 MCU BUSS BARS
MAIN BARS

NAME: DAVE KLINE

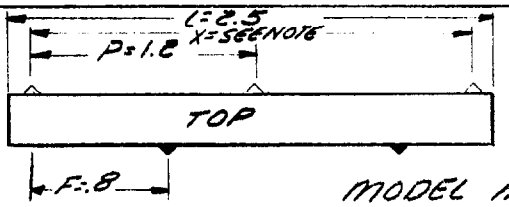
DATE: 7/24/78

REVISION DATE:



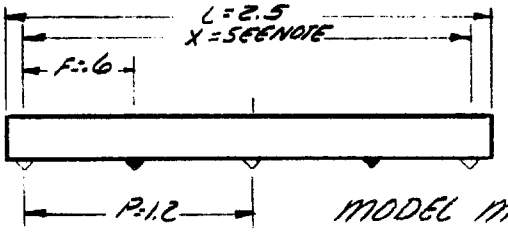
NOTE △ LAYER X=5
● LAYER X=4

MODEL M-822 (MODIFIED), ITEM 47 OF PARTS LIST



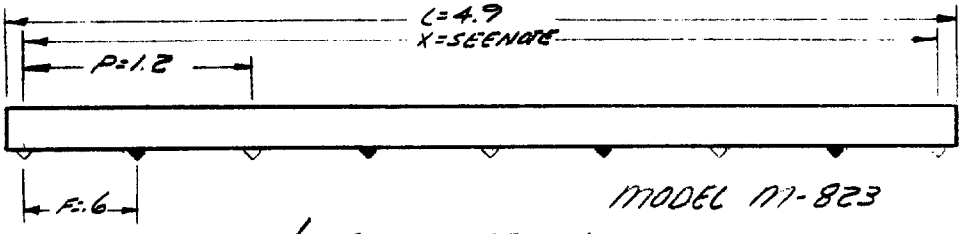
NOTE
△ LAYER X=2
● LAYER X=1

MODEL M-822 (MODIFIED), ITEM 48 OF PARTS LIST.



NOTE ▽ LAYER X=2
● LAYER X=1

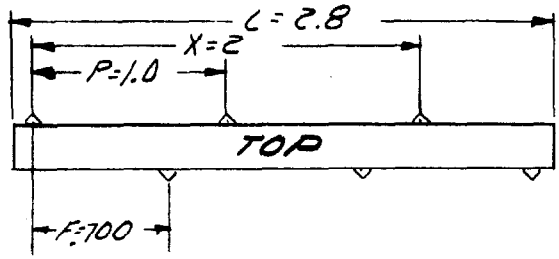
MODEL M-823 (MODIFIED), ITEM 49 OF PARTS LIST.



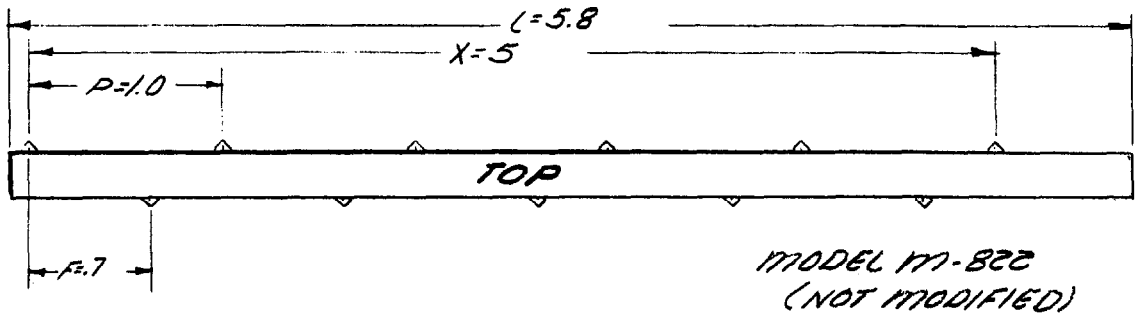
NOTE ▽ LAYER X=4
● LAYER X=3

MODEL M-823 MODIFIED, ITEM 50 OF PARTS LIST

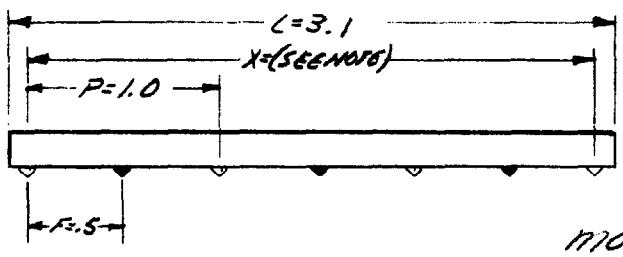
CONSULT FACTORY - THESE ARE SEMI-CUSTOM DESIGNS



MODEL M-822
(NOT MODIFIED)
(4 PER MLU)



MODEL M-822
(NOT MODIFIED)
(3 PER MLU)



MODEL M-823
(MODIFIED)

△ LAYER X=3

▲ LAYER X=2

SUBJECT: DOCUMENTATION OF: ECL-2

NAME: H. James Krebs

DATE: 11-29-78 | REVISION DATE:

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-EE-104292
FRONT PANEL MACHING DRAWING	0880-MC-104294
FRONT PANEL ASSEMBLY	0880-MC-104440
FRONT PANEL ARTWORK	0880-MC-104296
MODULE FINAL ASSEMBLY	0880-MD-104441
P.C. CARD COMPONENT ASSEMBLY (R.H.)	0880-MD-104442
P.C. CARD DRILL DRAWING (R.H.)	0880-MD-104443
P.C. CARD PARTS LIST (R.H.)	0880-MA-104444
P.C. CARD MASTER ARTWORK (R.H.)	0880-MD-104420
BOARD OUTLINE (R.H.)	0880-MC-104449
P.C. CARD COMPONENT ASSEMBLY (L.H.)	0880-MD-104445
P.C. CARD DRILL DRAWING (L.H.)	0880-MD-104446
P.C. CARD PARTS LIST (L.H.)	0880-MA-104447
P.C. CARD MASTER ARTWORK (L.H.)	0880-MD-104421
PHOTO REDUCTIONS	FP-30
BOARD OUTLINE (L.H.)	0880-MC-104448
SOFTWARE	

ECL/CAMAC TEST MODULE ECL-3

(General Purpose Test Module -

Wire Wrapped - Double Width)

General Description

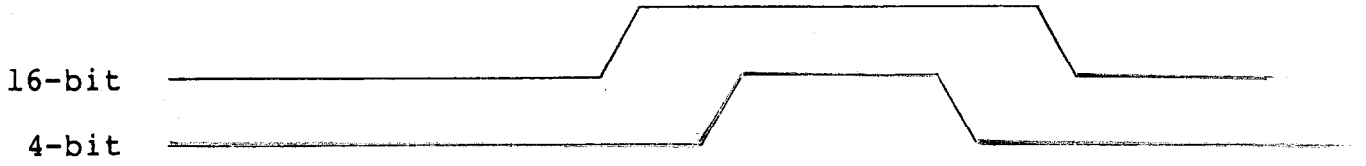
This module is designed to act as a test device for functional modules residing in an ECL/CAMAC crate.

The unit has an ECL/CAMAC accessable 16-bit and 4-bit output register and corresponding 16-bit and 4-bit input ports. The 16-bit register and port are interfaced thru 34 pin flat ribbon cable connectors on the front panel. The 4-bit register and port are interfaced thru front panel 2 pin LEMO connectors. Front panel LEDs statically display the state of all input/output bits.

The module is designed to be connected directly to devices such as the Memory Look-Up Module (MLU) (ECL-2) by means of flat ribbon cable for "ADDRESS OUT" and "DATA IN" and by LEMO terminated twisted pair cable for "READY OUT" and "READY IN".

Operating Modes

The ECL-3 operates in two (2) modes, local and remote. In local, an internal timer enables the contents of the 16-bit register first, then enables and disables the contents of the 4-bit register, then disables the 16-bit register. Data output is whatever was last loaded into the registers.



The cycle repeats itself ocntinuously as long as the mode switch is in the local position.

In the remote mode, the output registers are enabled at 11 times. All bit changes are executed by writing to the module via ECL/CAMAC.

CAMAC Function Codes

F16 A0 S1 Load the 16-bit output register

MSB XXXX XXXX XXXX XXXX LSB
R/W16 R/W1

F17 A0 S1 Load the 4-bit ouptut register

MSB XXXX LSB
R/W4 R/W1

F0 A0 Read the 16-bit input port

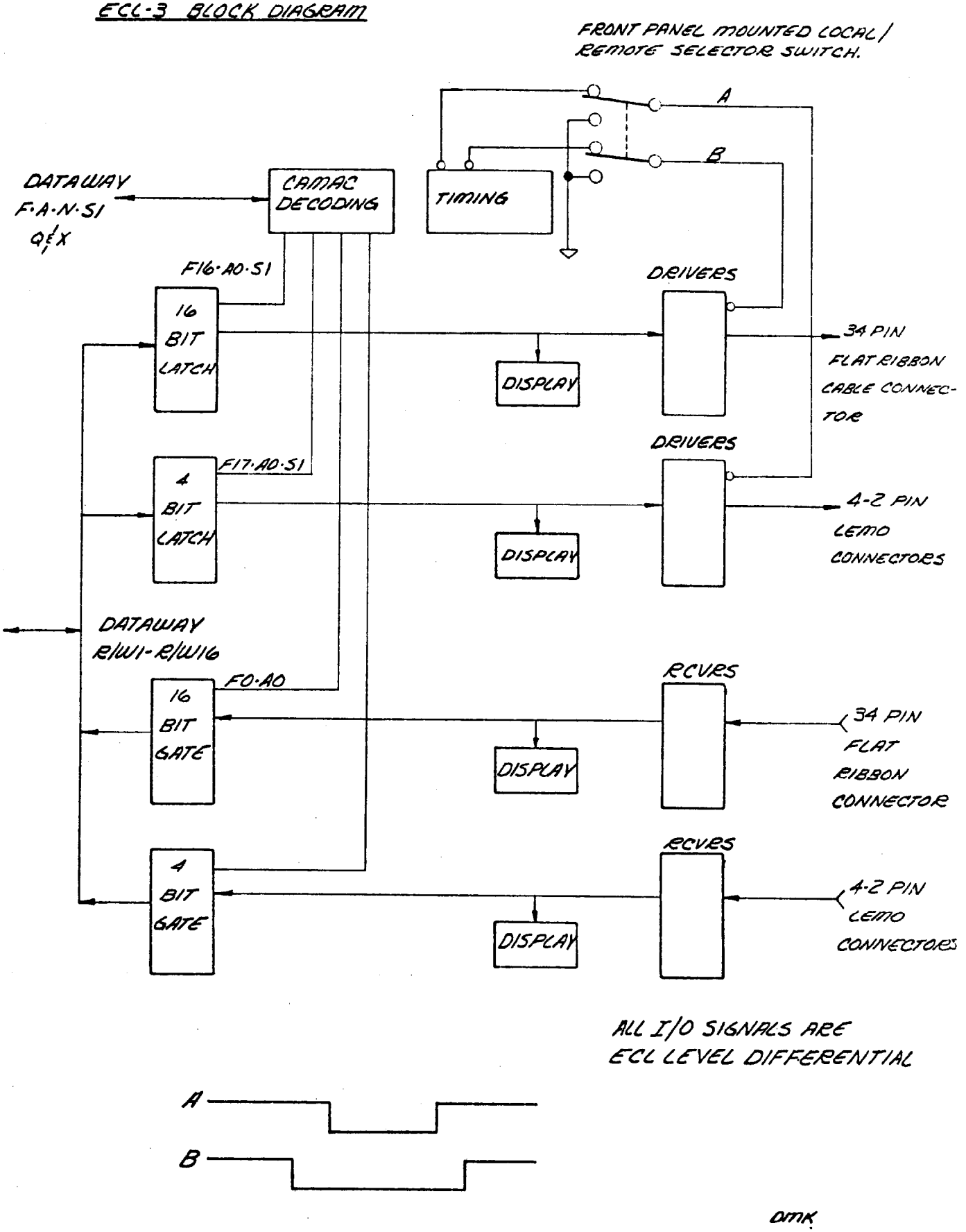
MSB XXXX XXXX XXXX XXXX LSB
R/W16 R/W1

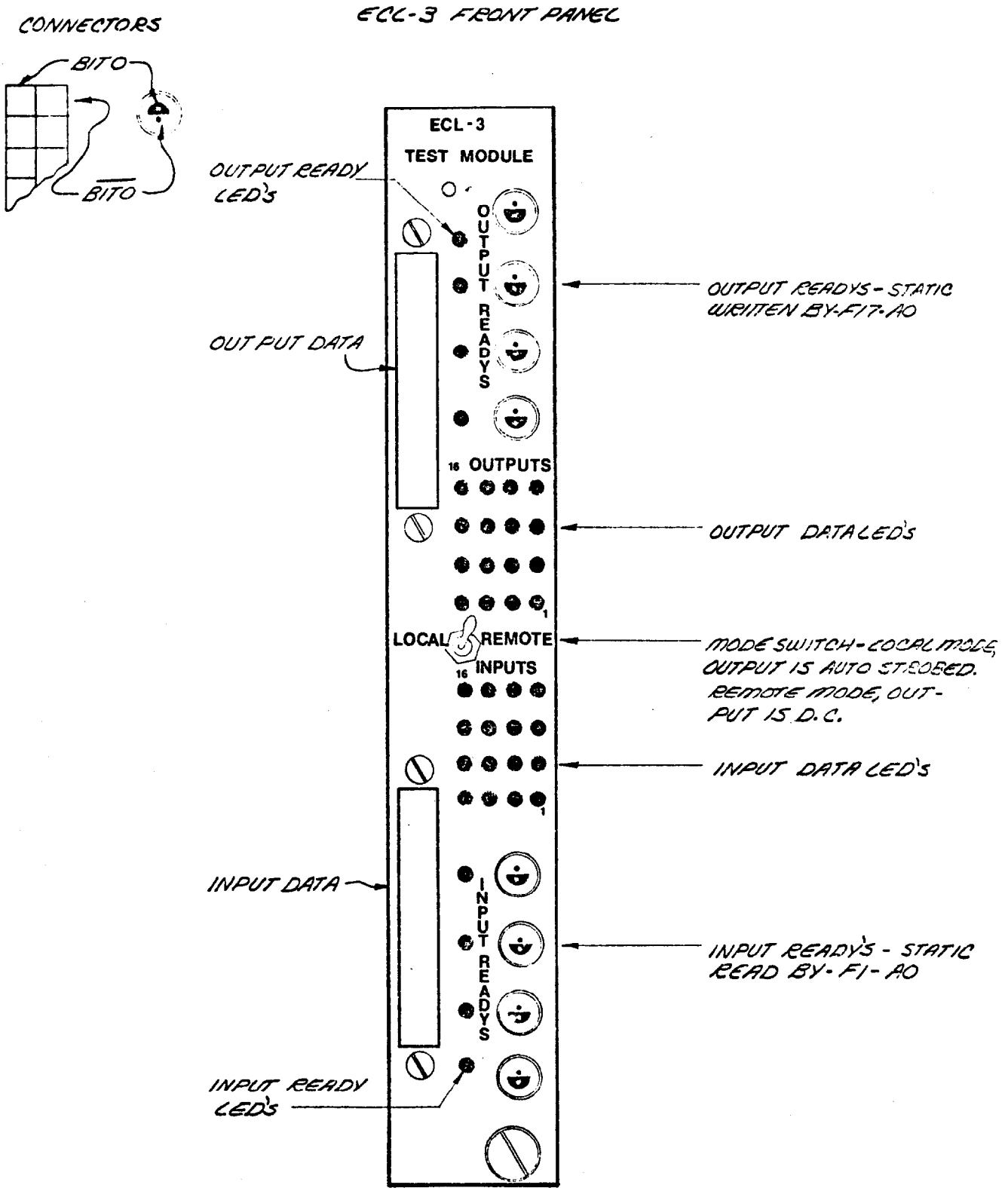
F1 A0 Read the 4-bit input port

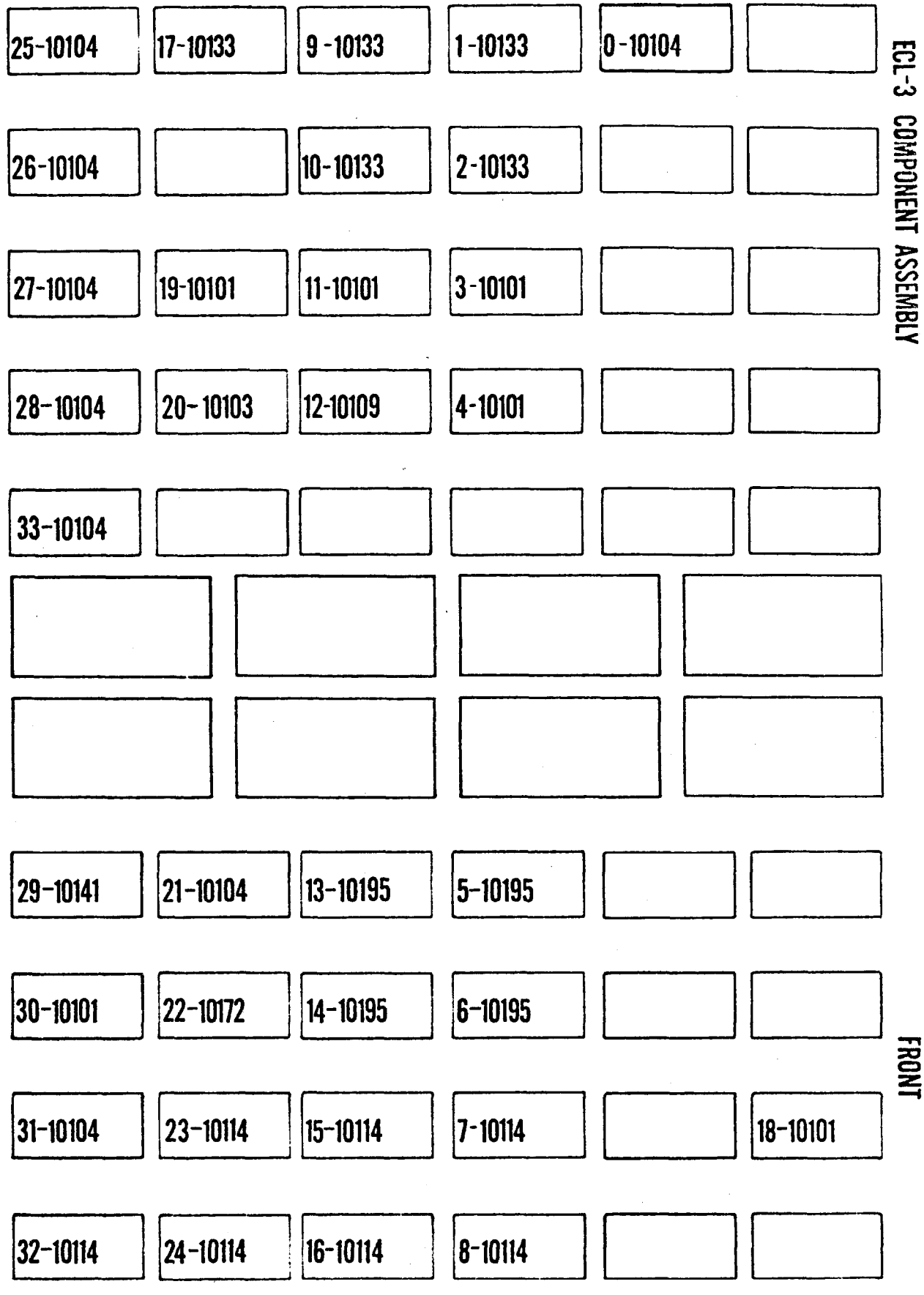
MSB XXXX LSB
R/W4 R/W1

(Prepared by R. Hance, February 1, 1978)

ECL-3 BLOCK DIAGRAM




CONNECTORS
BIT 0
BIT 0
ECL-3 FRONT PANEL
ECL-3
TEST MODULE
OUTPUT READY LED's
OUTPUT READYS
OUT PUT DATA
16 OUTPUTS
OUTPUT READYS - STATIC WRITTEN BY-F17-A0
OUTPUT DATA LED's
LOCAL
REMOTE
16 INPUTS
MODE SWITCH - LOCAL MODE, OUTPUT IS AUTO STROBED. REMOTE MODE, OUTPUT IS D.C.
INPUT DATA LED's
INPUT DATA
INPUT READYS
INPUT READY'S - STATIC READ BY - F1 - A0
INPUT READY LED's


25-10104
17-10133
9 -10133
1-10133
0-10104
26-10104
10-10133
2-10133
27-10104
19-10101
11-10101
3-10101
28-10104
20-10103
12-10109
4-10101
33-10104
29-10141
21-10104
13-10195
5-10195
30-10101
22-10172
14-10195
6-10195
31-10104
23-10114
15-10114
7-10114
18-10101
32-10114
24-10114
16-10114
8-10114
ECL-3 COMPONENT ASSEMBLY
FRONT

FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	Exp. 516	TM-0821	56

SUBJECT

DOCUMENTATION OF: ECL-3

NAME: H. James Krebs

DATE: 6-22-78

REVISION DATE:

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-ED-104337
FRONT PANEL MACHING DRAWING	0880-MC-104291
FRONT PANEL ASSEMBLY	0880-MC-104450
FRONT PANEL ARTWORK	
MODULE FINAL ASSEMBLY	
P.C. CARD COMPONENT ASSEMBLY	
P.C. CARD DRILL DRAWING	
P.C. CARD PARTS LIST	0880-MA-104451
P.C. CARD MASTER ARTWORK	
BOARD OUTLINE	

ECL/CAMAC Module ECL-4

Memory Stack

(General Purpose - Double Width - Multiwire PC Board)

As illustrated in the block diagram, the Stack is made up of a RAM with storage capacity of 32 16-bit words. The RAM is a single access device made to appear to have dual access by the associated logic.

Data to be written to the stack is fed into the Write Data (WD) input and accepted when Sequential Write Ready (SWR) goes high.

Data to be read from the Stack comes from the Read Data (RD) output and is considered valid when Output Ready (OR) goes high. A signal at the Sequential Read Ready (SRR) input is used to read the stack at an address determined by the internal read address register whereas a Random Read Ready (RRR) is used when the desired address to be read is input at Read Address (RA), (A signal on RRR sets the internal read address register to zero).

The Read Inhibit (RI) input is used to inhibit SRR's and RRR's; allowing one to write an uninterrupted block of words to the stack. If RI is not used SRR, RRR and SWR are handled on an established priority basis which is as follows: During a READ, WRITE has priority and during a WRITE, READ has priority. If during a WRITE, both SRR and RRR occurred, RRR has priority though both will be serviced.

A Camac operation inhibits all input READYs during CAMAC writing and reading of the RAM, address registers and/or resetting the module.

The mode of operation can be modified by on-board jumpers and can be determined by looking at the flow charts and timing diagrams.

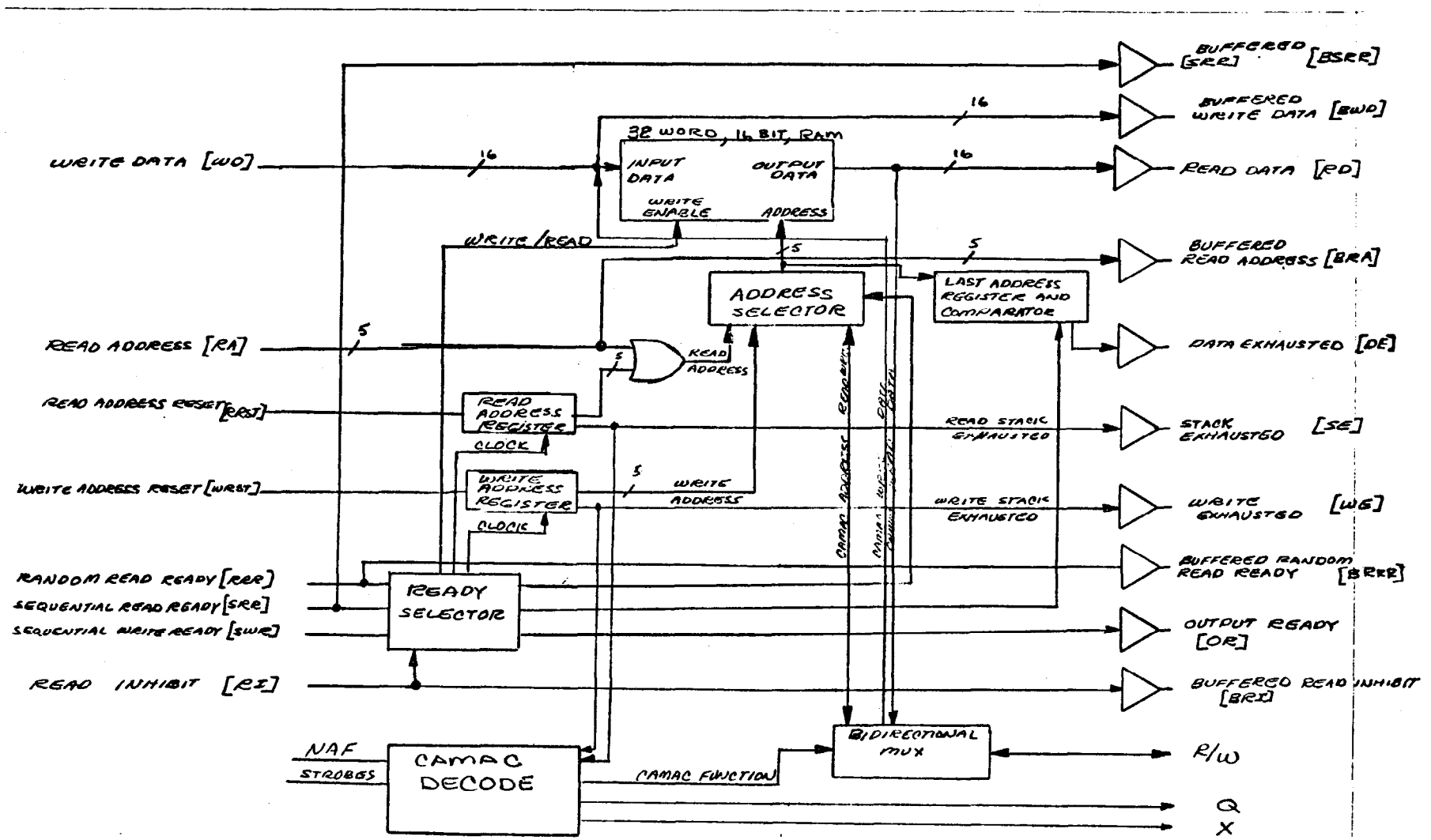
Several stacks may be combined to increase the number of words and/or bits. If, for example sixty four 16-bit words are to be stored; two stacks could be used with data (WD) and strobes (SWR) going to the first stack and the following connections between the 1st and 2nd stack:

From 1st	To 2nd
WE	RI
BSWR	SWR
BWD	WD

Of course parallel configurations (64 32-bit words etc.) can also be used.

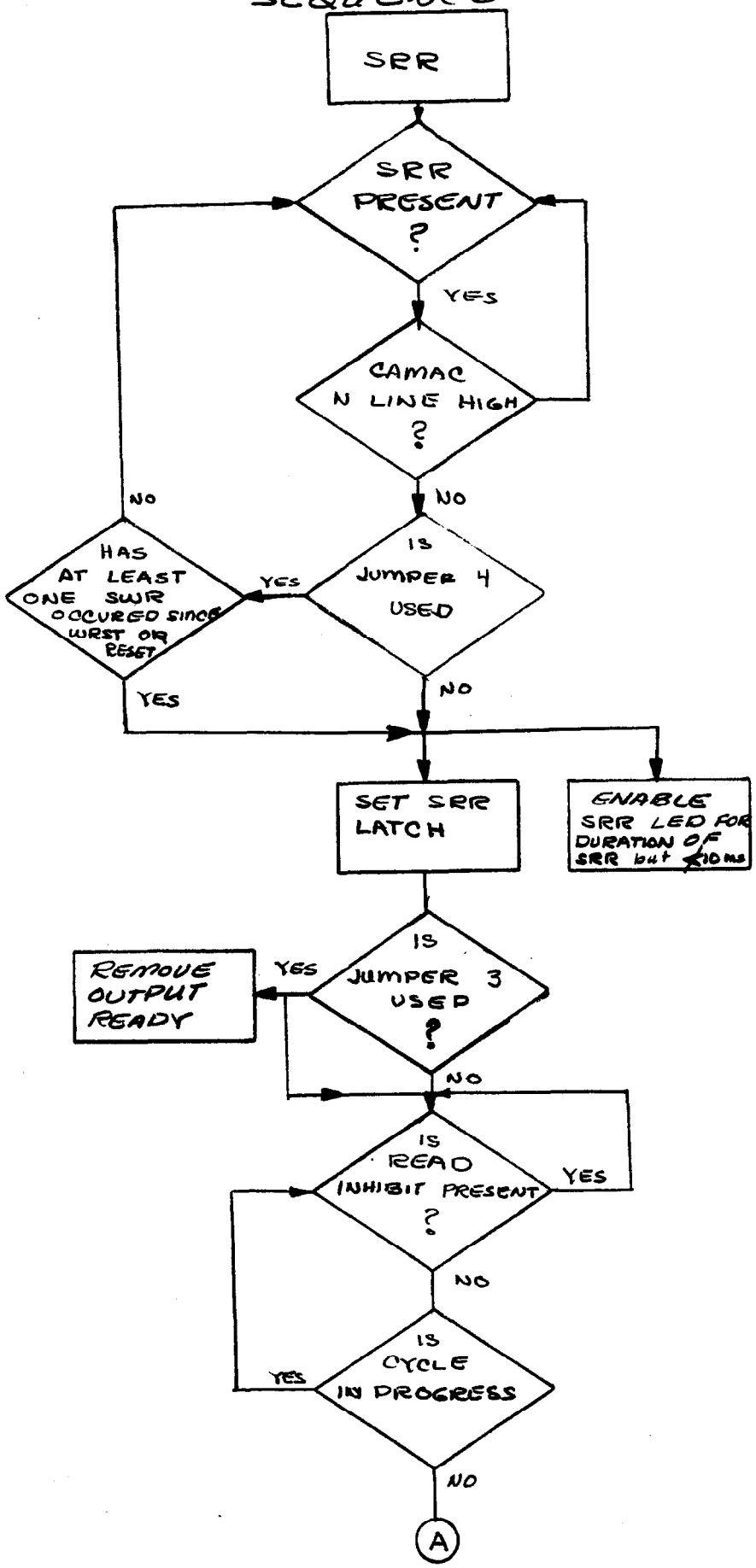
Additional outputs are available such as data exhausted (DE) which indicates an attempt has been made to read data at an address beyond the last written address, and stack exhausted (SE) which indicates an attempt has been made to read beyond the 32-word capacity. See the flow charts and timing diagrams for more details.

(Prepared by M. Haldeman and B. Haynes, 10/78)

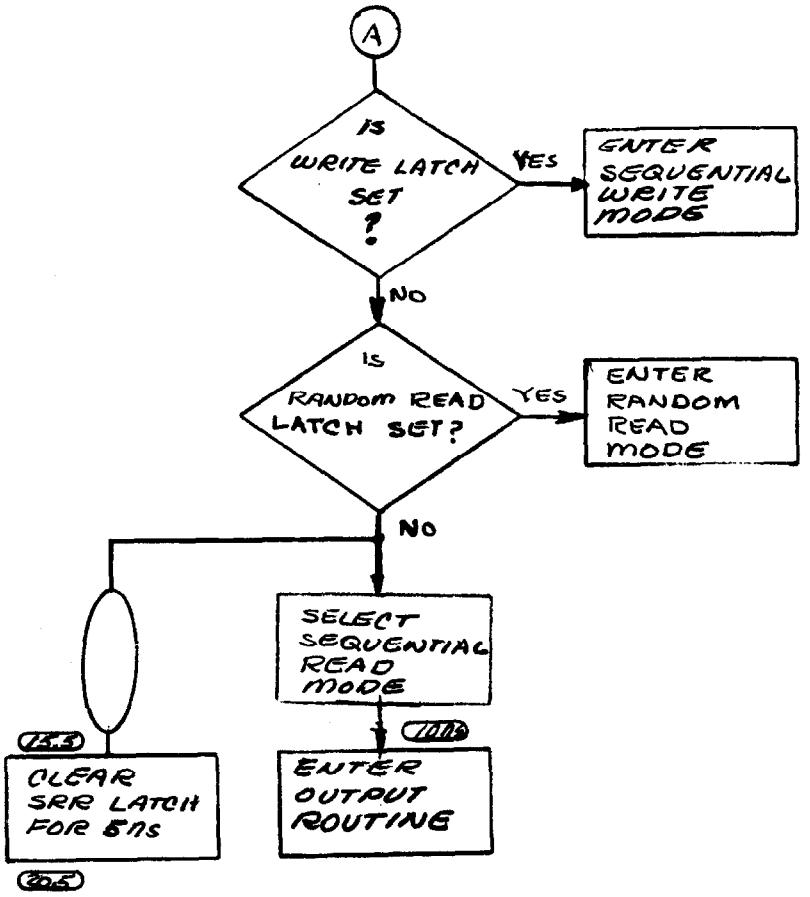


BLOCIC DIAGRAM

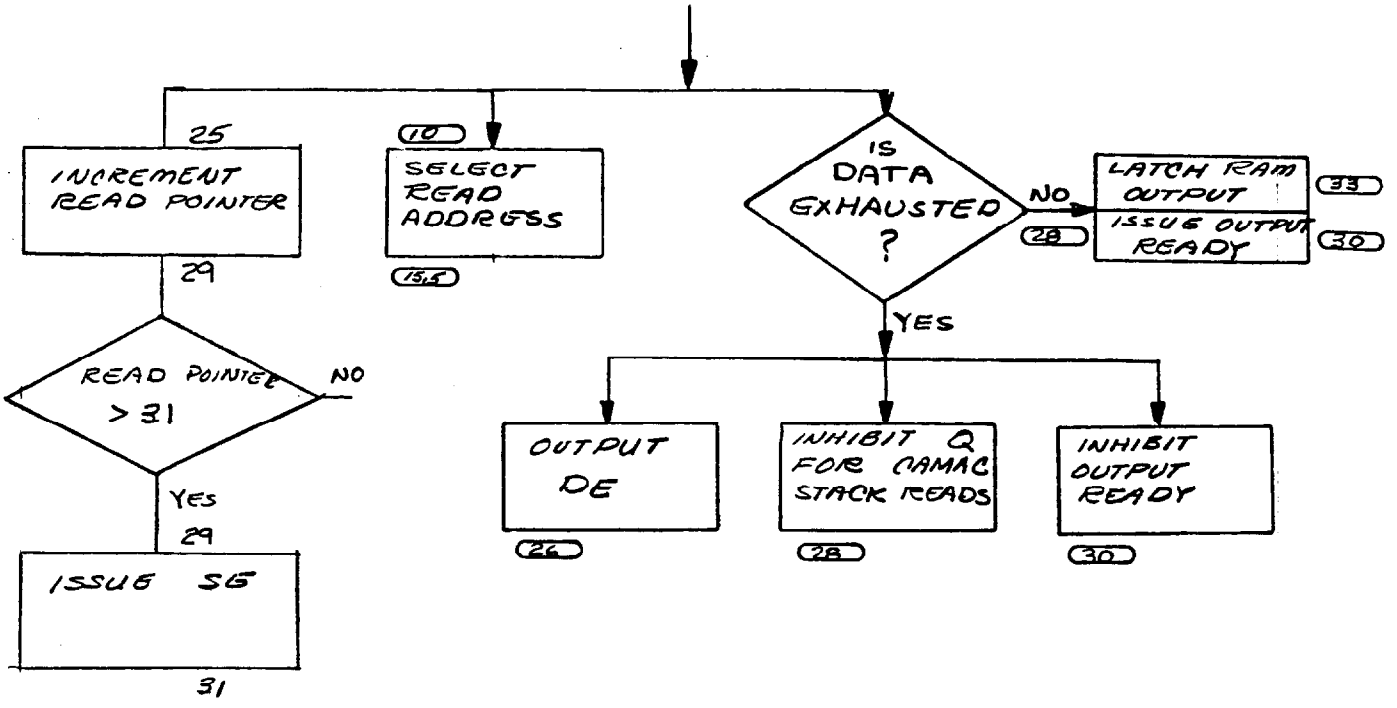
GENERAL SEQUENTIAL READ SEQUENCE



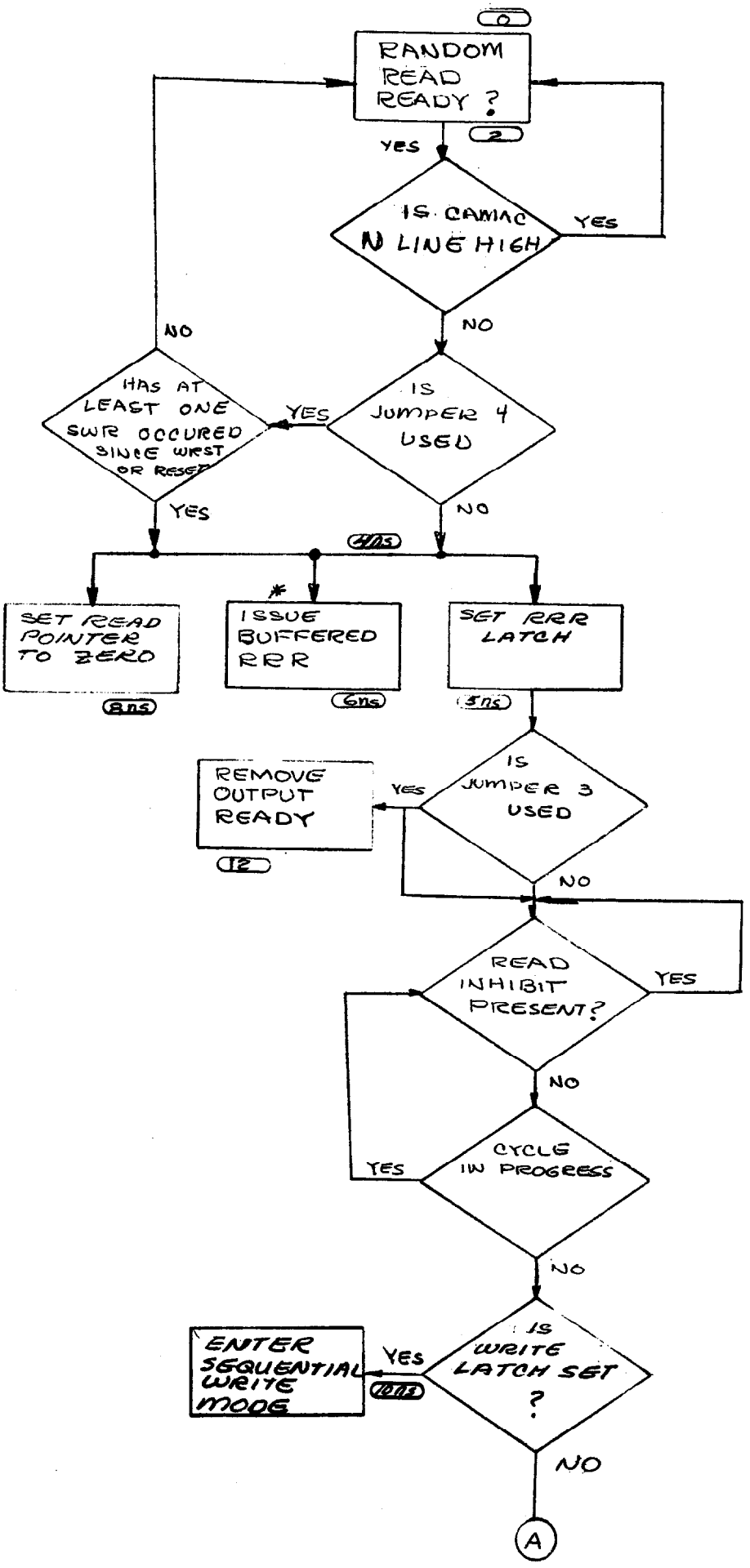
SEQUENTIAL READ CONTINUED



OUTPUT ROUTING

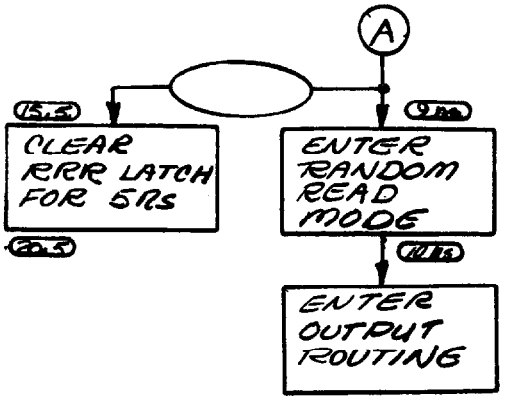


RANDOM READ SEQUENCE

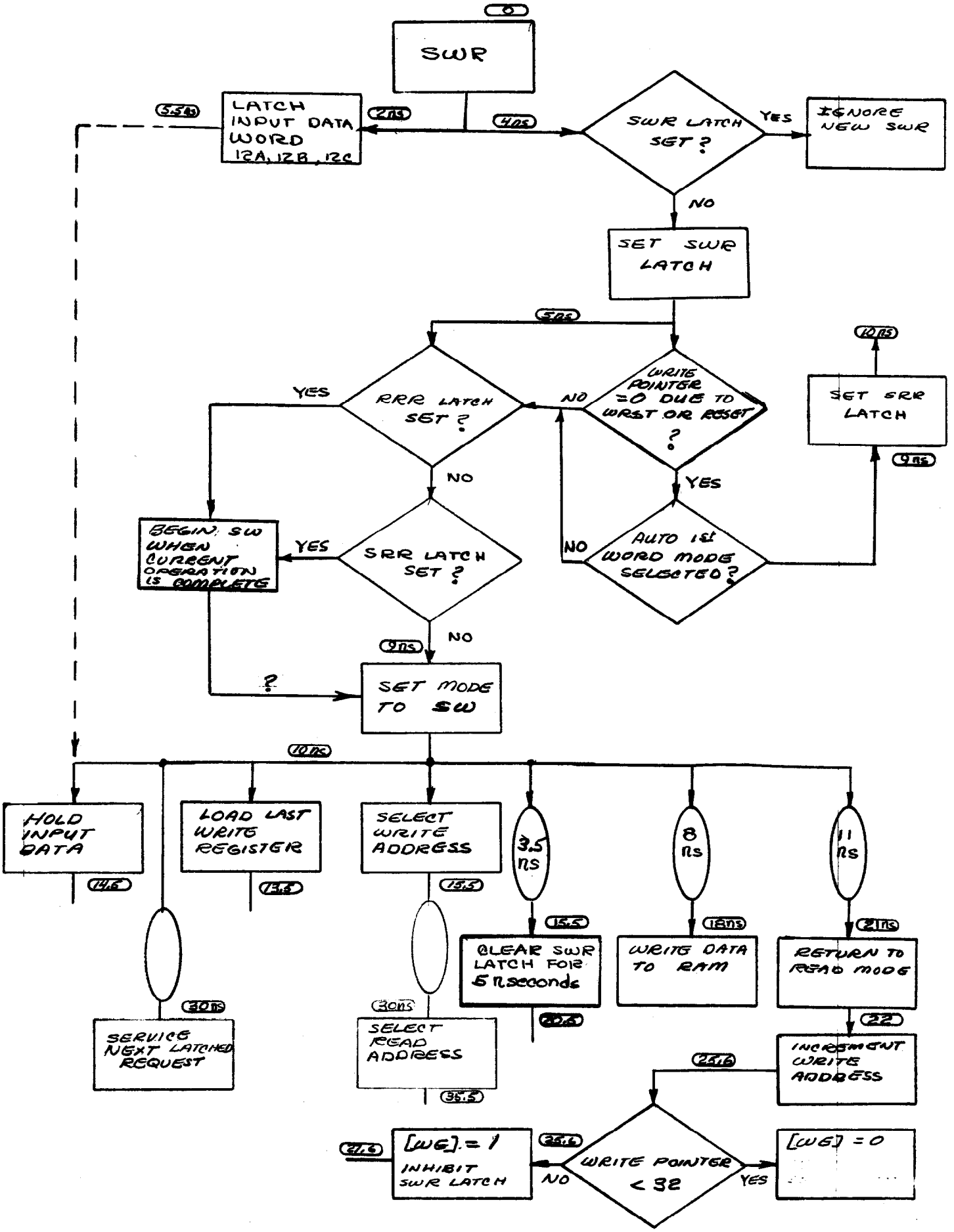


* CHANGES TO BE MADE

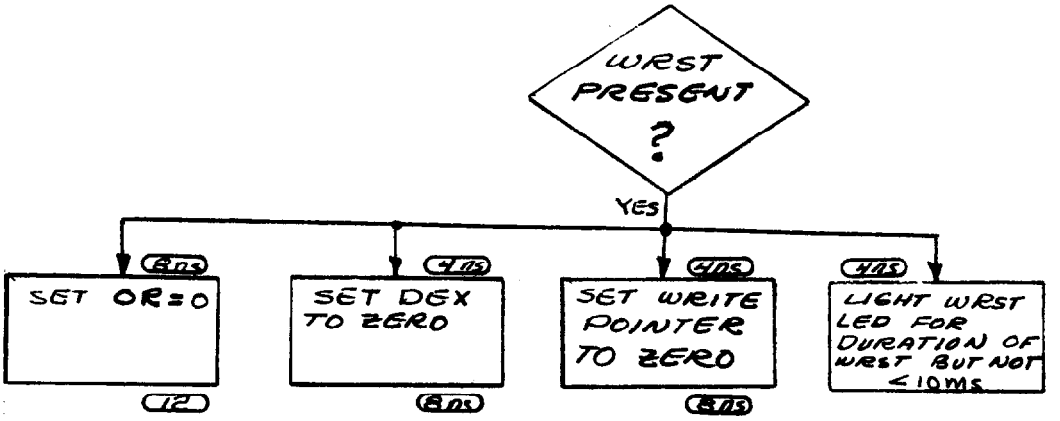
RANDOM
READ
CONTINUED



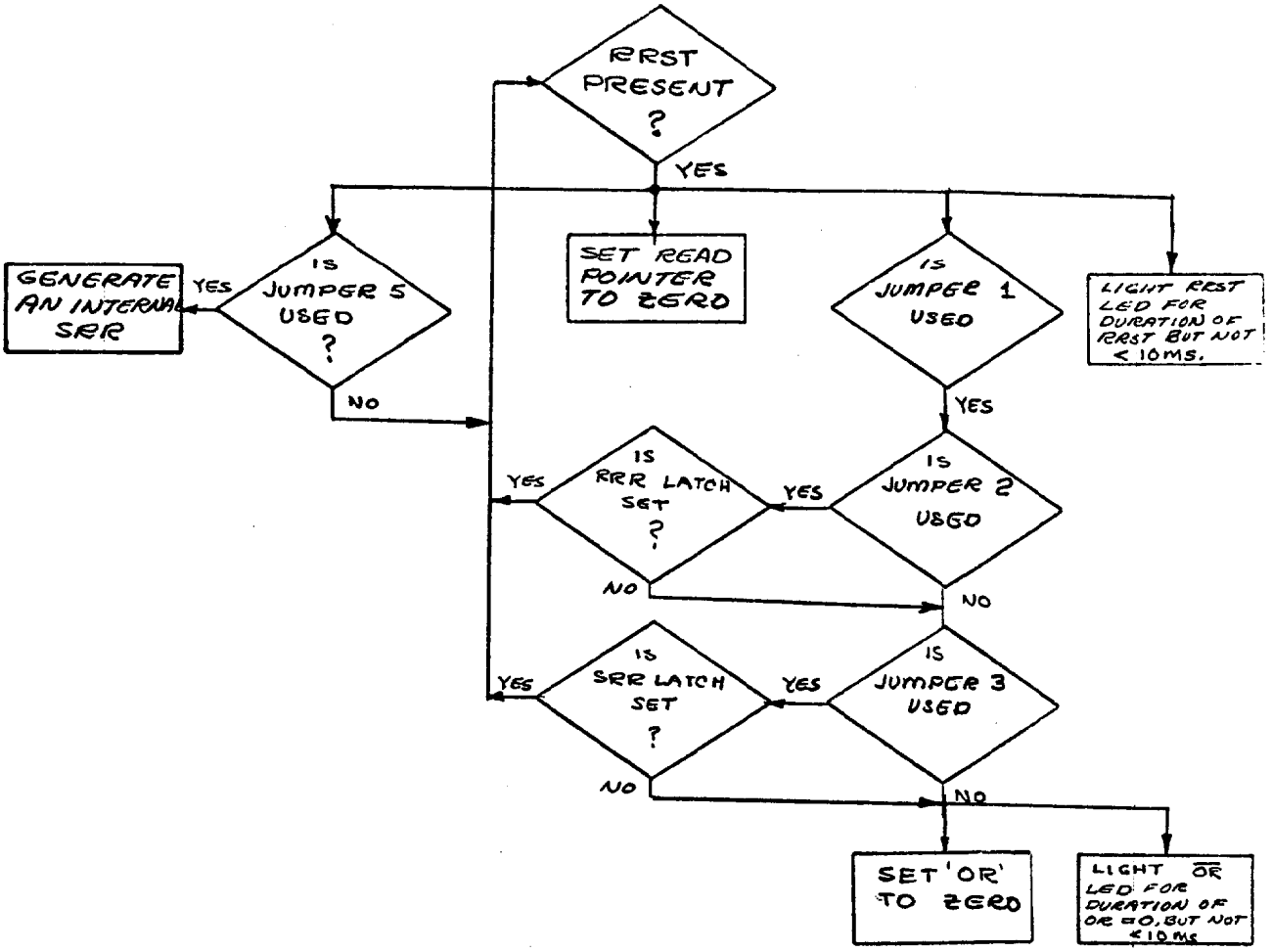
GENERAL SEQUENTIAL WRITE SEQUENCE.



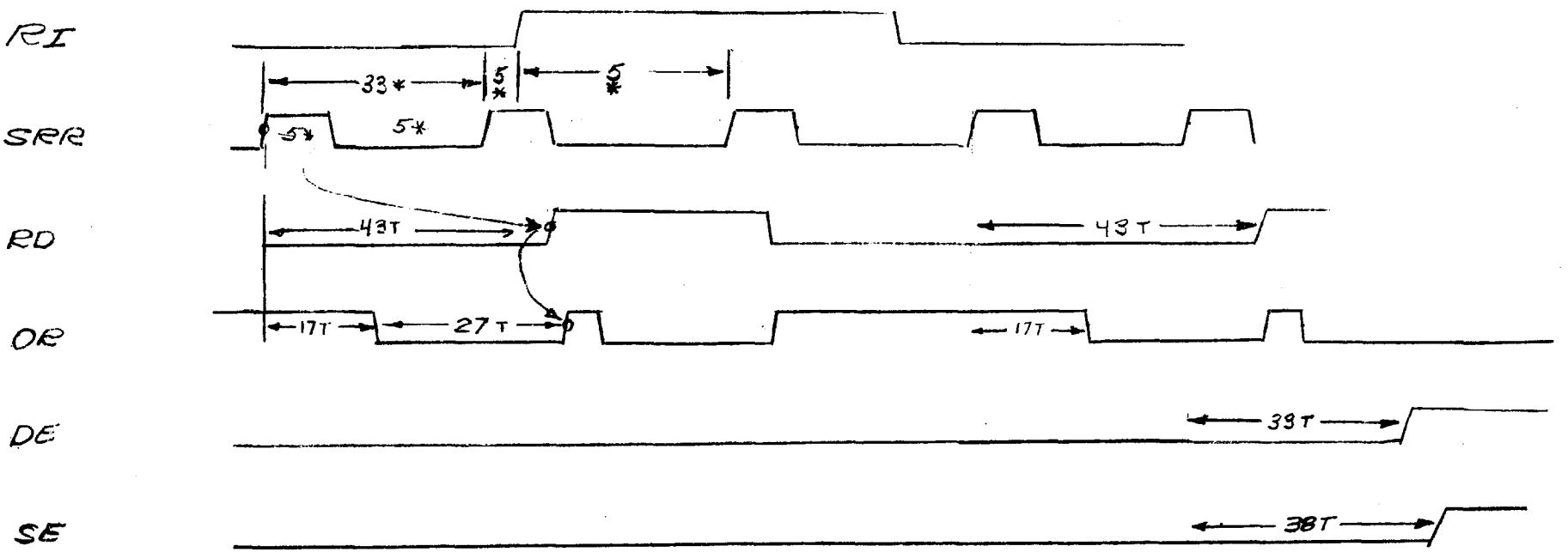
WRITE ADDRESS RESET



READ ADDRESS RESET



SEQUENTIAL READ TIMING DIAGRAM



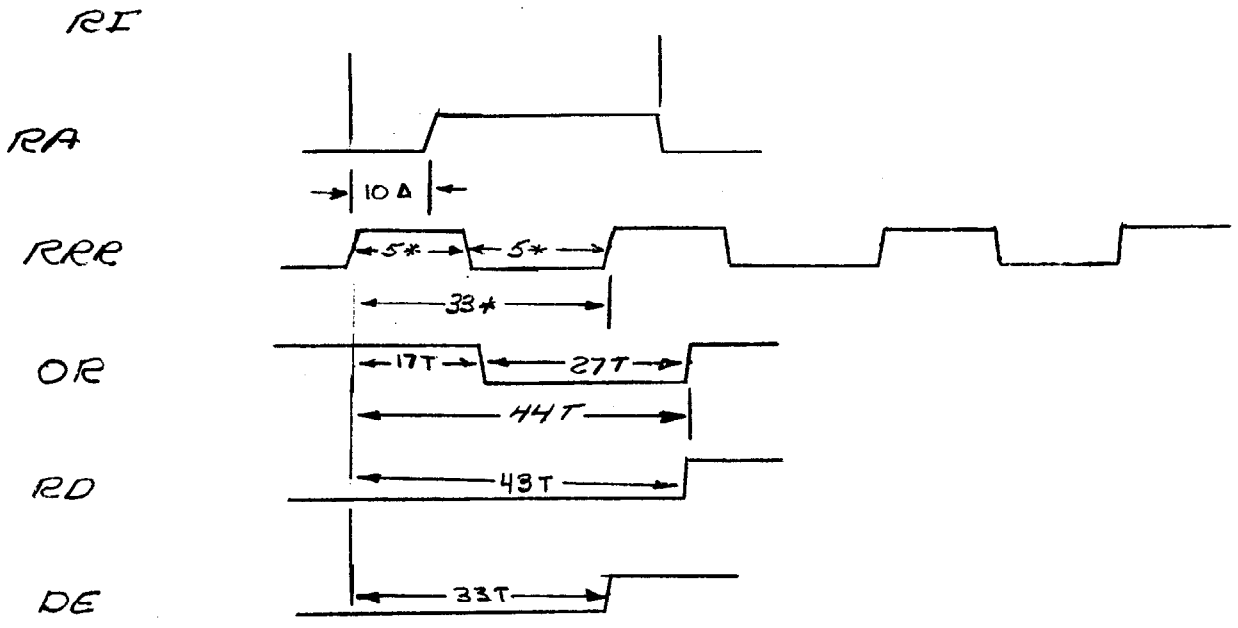
ALL TIMES ARE IN NANO SECONDS

* = MIN

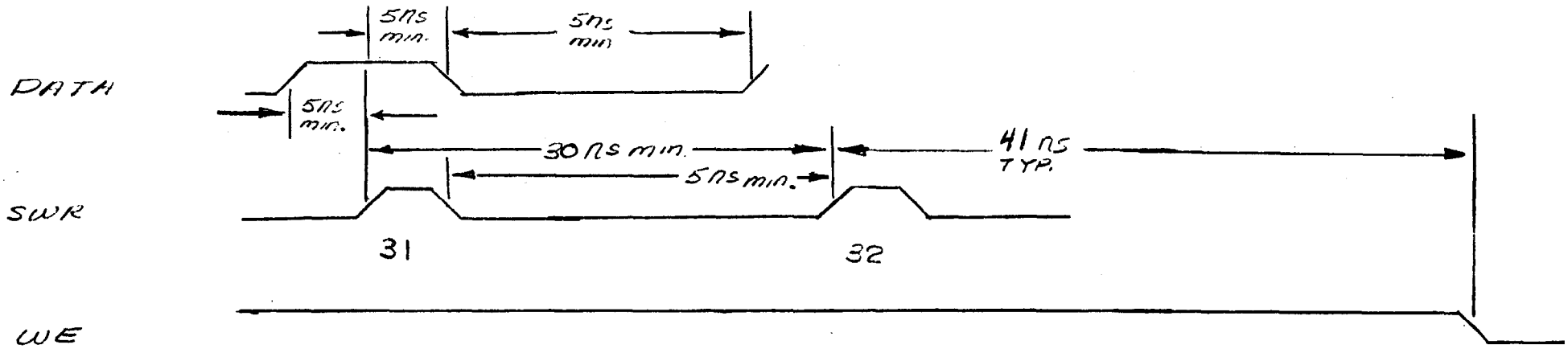
Δ = MAX

T = TYP

RANDOM READ TIMING DIAGRAM



SEQUENTIAL WRITE TIMING DIAGRAM



(10139) ECL-4 (IF)

C3 (XXX) 256 BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: _____
P.O. NO.: _____
YOUR PART NO.: _____
DATE: _____

THIS PORTION TO BE COMPLETED BY SIGNETICS
PART NO.: _____
S.D. NO.: _____
DATE RECEIVED: _____

	WORD	INPUTS						OUTPUTS							
		A_4	A_3	A_2	A_1	A_0	ENABLE	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
F0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	1	0	0	0	0	1	0								
	2	0	0	0	1	0	0								
	3	0	0	0	1	1	0								
	4	0	0	1	0	0	0								
	5	0	0	1	0	1	0								
	6	0	0	1	1	0	0								
	7	0	0	1	1	1	0								
F16	8	0	1	0	0	0	0	0	0	0	0	1	0	0	0
	9	0	1	0	0	1	0								
	10	0	1	0	1	0	0								
	11	0	1	0	1	1	0								
	12	0	1	1	0	0	0								
	13	0	1	1	0	1	0								
	14	0	1	1	1	0	0								
	15	0	1	1	1	1	0								
F0	16	1	0	0	0	0	0	0	0	0	0	0	1	0	0
F1	17	1	0	0	0	1	0	0	0	0	0	0	1	0	1
F2	18	1	0	0	1	0	0	0	0	0	0	0	1	1	0
F3	19	1	0	0	1	1	0	0	0	0	0	0	1	1	1
	20	1	0	1	0	0	0								
	21	1	0	1	0	1	0								
	22	1	0	1	1	0	0								
	23	1	0	1	1	1	0								
F16	24	1	1	0	0	0	0	0	0	0	0	1	0	0	0
F17	25	1	1	0	0	1	0	0	0	0	0	1	0	0	0
F18	26	1	1	0	1	0	0	0	0	0	0	1	0	0	0
	27	1	1	0	1	1	0								
	28	1	1	1	0	0	0								
	29	1	1	1	0	1	0								
	30	1	1	1	1	0	0								
	31	1	1	1	1	1	0								
	ALL	X	X	X	X	X	1	1	1	1	1	1 F1+ F2+ F16	1 F0+ F1+ F3	1 F2+ F3	1 F1+ F0

(10139) ECC-4 (16)

CS (XXX) 256 BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: _____ THIS PORTION TO BE COMPLETED BY SIGNETICS

P.O. NO.: _____ PART NO.: _____

YOUR PART NO.: _____ S.D. NO.: _____

DATE: _____ DATE RECEIVED: _____

	WORD	INPUTS						OUTPUTS							
		A_4	A_3	A_2	A_1	A_0	ENABLE	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
F0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
	1	0	0	0	0	1	0								
	2	0	0	0	1	0	0								
	3	0	0	0	1	1	0								
	4	0	0	1	0	0	0								
	5	0	0	1	0	1	0								
	6	0	0	1	1	0	0								
	7	0	0	1	1	1	0								
F16	8	0	1	0	0	0	0	0	0	0	1	0	0	1	0
	9	0	1	0	0	1	0								
	10	0	1	0	1	0	0								
	11	0	1	0	1	1	0								
	12	0	1	1	0	0	0								
	13	0	1	1	0	1	0								
	14	0	1	1	1	0	0								
	15	0	1	1	1	1	0								
F0	16	1	0	0	0	0	0	0	0	0	0	0	1	1	0
F1	17	1	0	0	0	1	0	0	0	0	0	0	0	1	1
FC	18	1	0	0	1	0	0	0	0	0	0	0	0	1	1
F3	19	1	0	0	1	1	0	0	0	0	0	0	0	1	1
	20	1	0	1	0	0	0								
F9	21	1	0	1	0	1	0	0	0	0	0	1	0	1	1
	22	1	0	1	1	0	0								
	23	1	0	1	1	1	0								
F16	24	1	1	0	0	0	0	0	0	0	1	0	0	1	0
F17	25	1	1	0	0	1	0	0	0	1	0	0	0	1	1
F18	26	1	1	0	1	0	0	0	1	0	0	0	0	1	1
	27	1	1	0	1	1	0								
	28	1	1	1	0	0	0								
F25	29	1	1	1	0	1	0	1	0	0	0	0	0	1	1
	30	1	1	1	1	0	0								
	31	1	1	1	1	1	0								
	ALL	X	X	X	X	X	1	1 F25	1 F16	1 F17	1 F16	1 F9	1 F0	1 X'	1 Q'

ECL-A

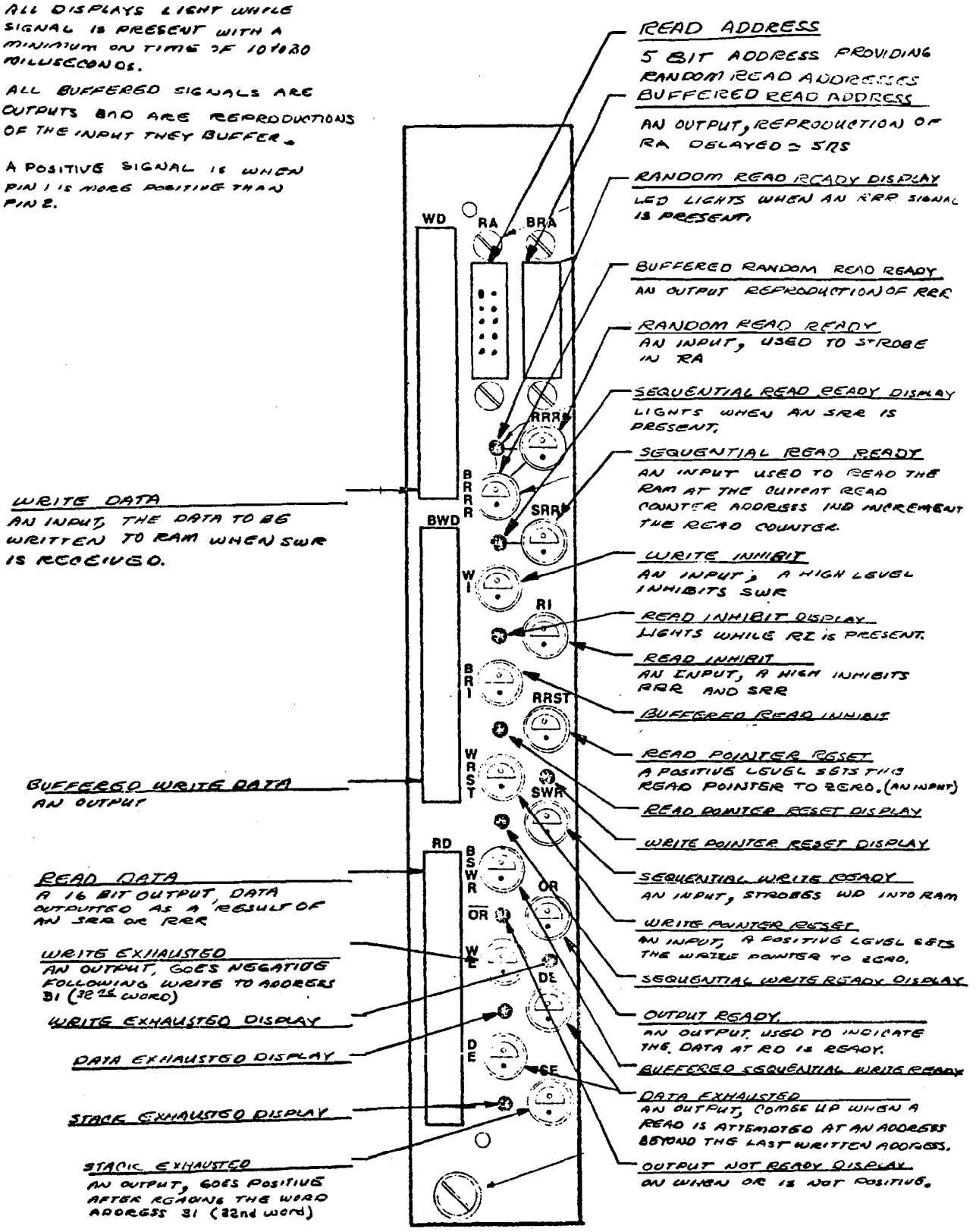
RESPONSE		CODES	FUNCTION
X	Q		
/	*	F0·AX	READ STACK DATA
/	/	F1·A0	READ STACK READ POINTER
/	/	FC·A0	READ STACK WRITE POINTER
/	/	F3·A0	READ LAST WRITTEN ADDRESS
/	/	F9·A0·S1	RESET
/	**	F16·AX·S1	WRITE STACK DATA
/	/	F17·A0·S1	WRITE STACK READ POINTER
/	/	F18·A0·S1	WRITE STACK WRITE POINTER
/	/	FC5·A0·S1	TRANSFER WRITE POINTER TO LAST WRITTEN ADDRESS REGISTER.

$*= 1IF,\ N\cdot F0\cdot AX\cdot \overline{ESEX}' = \overline{DEX}$

$**= 1IF,\ N\cdot F16\cdot AX\cdot \overline{WSEX}'$

NOTES:

1. ALL DISPLAYS LIGHT WHILE SIGNAL IS PRESENT WITH A MINIMUM ON TIME OF 10 TO 30 MILLISECONDS.
2. ALL BUFFERED SIGNALS ARE OUTPUTS AND ARE REPRODUCTIONS OF THE INPUT THEY BUFFER.
3. A POSITIVE SIGNAL IS WHEN PIN 1 IS MORE POSITIVE THAN PIN 2.



READ ADDRESS
5 BIT ADDRESS PROVIDING RANDOM READ ADDRESSES

BUFFERED READ ADDRESS
AN OUTPUT, REPRODUCTION OF RA DELAYED ≃ 5nS

RANDOM READ READY DISPLAY
LED LIGHTS WHEN AN RRR SIGNAL IS PRESENT.

BUFFERED RANDOM READ READY
AN OUTPUT REPRODUCTION OF RRR

RANDOM READ READY
AN INPUT, USED TO STROBE IN RA

SEQUENTIAL READ READY DISPLAY
LIGHTS WHEN AN SRR IS PRESENT.

SEQUENTIAL READ READY
AN INPUT USED TO READ THE RAM AT THE CURRENT READ COUNTER ADDRESS AND INCREMENT THE READ COUNTER.

WRITE DATA
AN INPUT, THE DATA TO BE WRITTEN TO RAM WHEN SWR IS RECEIVED.

WRITE INHIBIT
AN INPUT, A HIGH LEVEL INHIBITS SWR

READ INHIBIT DISPLAY
LIGHTS WHILE RI IS PRESENT.

READ INHIBIT
AN INPUT, A HIGH INHIBITS RRR AND SRR

BUFFERED READ INHIBIT

READ POINTER RESET
A POSITIVE LEVEL SETS THE READ POINTER TO ZERO. (AN INPUT)

BUFFERED WRITE DATA
AN OUTPUT

READ POINTER RESET DISPLAY

WRITE POINTER RESET DISPLAY

SEQUENTIAL WRITE READY
AN INPUT, STROBES WD INTO RAM

READ DATA
A 16 BIT OUTPUT, DATA OUTPUTTED AS A RESULT OF AN SRR OR RRR

WRITE POINTER RESET
AN INPUT, A POSITIVE LEVEL SETS THE WRITE POINTER TO ZERO.

WRITE EXHAUSTED
AN OUTPUT, GOES NEGATIVE FOLLOWING WRITE TO ADDRESS 31 (32nd WORD)

SEQUENTIAL WRITE READY DISPLAY

WRITE EXHAUSTED DISPLAY

OUTPUT READY
AN OUTPUT, USED TO INDICATE THE DATA AT RD IS READY.

DATA EXHAUSTED DISPLAY

BUFFERED SEQUENTIAL WRITE READY

STACK EXHAUSTED DISPLAY

DATA EXHAUSTED
AN OUTPUT, COMES UP WHEN A READ IS ATTEMPTED AT AN ADDRESS BEYOND THE LAST WRITTEN ADDRESS.

STACK EXHAUSTED
AN OUTPUT, GOES POSITIVE AFTER READING THE WORD ADDRESS 31 (32nd word)

OUTPUT NOT READY DISPLAY
ON WHEN OR IS NOT POSITIVE.

SUBJECT: DOCUMENTATION OF: ECL-4

NAME: H. James Krebs

DATE: 11-22-78 | REVISION DATE: 11-22-78

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-EE-104326
FRONT PANEL MACHING DRAWING	0880-MC-104331
FRONT PANEL ASSEMBLY	0880-MC-104333
FRONT PANEL ARTWORK	0880-MC-104332
MODULE FINAL ASSEMBLY	0880-MD-104334
P.C. CARD COMPONENT ASSEMBLY	0880-MD-104388
P.C. CARD SILKSCREEN ARTWORK	0880-MD-104389
MODULE PARTS LIST	0880-MA-104392
P.C. CARD MASTER ARTWORK (POWER & GROUND)	0880-MD-104390
BOARD OUTLINE	0880-MC-104391
PHOTO REDUCTIONS	FP-31
MULTIWIRE, IBM CARD DECK	

ECL/CAMAC MODULE ECL-6

PWC Data Receiver and Centroid Processor
(Limited Purpose Module - Wire Wrapped - Double Width)

This module and ECL 8, 9, 10 and 4 form the complete Track Finder Subsystem. A general description of how these modules are used together to find tracks may be found in the ECL9 section.

General Description

This module receives data transmitted over long (> 100 feet) cables from the Carleton University MWPC encoder transmitter according to Standard RS422. It routes data to the appropriate Z^{in} or Z^{out} stack (ECL 4), or to the Z^{mid} hit array in the Track Finder (ECL 9/10). In the latter case a CTS (Clear To Send) signal is first received from the Track Finder. It provides appropriate RDYs to the Stacks and Track Finder, RIs (Read Inhibit) to the Stacks and RTS (Request to Send) to the Track Finder.

The module scans the spread (number of wires on for a given address as transmitted from the MWPC Encoder) and depending on instructions loaded in a PROM will transmit 0-4 addresses to the Stacks or Track Finder. These addresses correspond to presumed

hit addresses. A wide hit (large spread) may thus be interpreted as more than 1 hit. For example, we expect that typical spread for a single hit of induced anode readout of the E516 recoil MWPC will be 3. Thus the following instructions might be loaded in the PROM (where Z_o = centroid)

Spread	Presumed Hits
1	none
2	Z_o
3	Z_o
4	Z_o
5	Z_o-1, Z_o+1
6	$Z_o-\frac{3}{2}$, $Z_o+\frac{3}{2}$

Note that 1/2 wire precision is maintained on Z^{in} and Z^{out} (11 bits). Z^{mid} is rounded to 10 bits.

Only one address per presumed hit is loaded into the stacks (Z^{in}, Z^{out}). However in order to allow control of resolution in projecting PZ^{mid} into the hit array in the Track Finder, this module may transmit several addresses (Z^{mid}) for each presumed hit to the Track Finder. This is controlled by a PROM. A total of up to 16 addresses (Z^{mid}) may be sent for each mid-plane centroid/spread word from the encoder. The maximum range of addresses including voids permitted by a given PROM limits the rate at which this module can operate. If a full range of 16 is required then the MWPC transmitter must slow down to 1 full cycle (In, Mid, Out) time of > 500 nsec. If the range is ≤ 9 then a faster cycle time of > 300 nsec is acceptable. After

chamber alignment, etc., in E516 a resolution of 1 wire is expected. During startup resolution of 3 or more wires will be used to facilitate track finding.

INPUTS AND OUTPUTS

Inputs (All signals are ECL level differential except as indicated.)

PWC DATA TTL level, RS-422 standard data from the proportional wire chamber. Data includes centroid address, width, chamber number, start, stop and clock.

19	18	17	16 15	14 11	10 0
Clock	Start	Stop	Chamber	Spread	Centroid Address
	on during first word only	on while transmitting last word of each chamber	01 In 10 Mid 11 Out		

CTS Clear to send signal from the track finder J chamber hit array (ECL 9/10).

Reset Initializing signal from the ECL/CAMAC dataway. Single ended.

Power +6, -5.2, -2 Volts from the ECL/CAMAC dataway.

Outputs	Bits	
I DATA	11	Centroids to the I Chamber Hit Stack. (Z^{in} - inner chamber coordinate)
I RDY	1	Data strobe to the I Chamber Hit Stack.
I INH	1	Read inhibit signal to the I Chamber Hit Stack.
J DATA	10	Centroids to the Track Finder (ECL 9/10) J Chamber Hit Array. (Z^{mid} - mid chamber coordinate).
J RDY	1	Data strobe to the Track Finder J Chamber Hit Array.
J RTS	1	Request to send to the Track Finder J Chamber Hit Array.
K DATA	11	Centroids to the K Chamber Hit Stack. (Z^{out} - out chamber coordinate).
K RDY	1	Data strobe the K Chamber Hit Stack.
K INH	1	Read inhibit signal to the K chamber Hit Stack.
START	1	Start/finish signal to the track finder Do Loop Controller (ECL 8).

Processing Time

J chamber centroids take a minimum of 500 ns to process, and I or K centroids take a minimum of 150 ns to process. I or K centroids can be processed simultaneously with a J centroid providing at least 150 ns elapses between receipt of a J centroid, and receipt of an I or K centroid. Therefore, J centroids must be received no faster than one every 500 ns, and all centroids must be received no sooner than 150 ns after the one before it.

Operating Description

The parallel 19-bit data word is received from the PWC, converted from TTL to ECL logic levels and latched internally in the receiver. The chamber number is then decoded. It will be used to steer the centroid information to the proper destination. Simultaneously, the width (W) is evaluated by the preprogrammed Width PROM. This PROM decides how many coordinates will be created from the centroid (X) received, and how far apart they will be. As the PROM data becomes valid, an arithmetic operation is taking place where the derived offset gets subtracted from the received centroid address. For any width (W) the PROM is programmed with control bits that result in coordinate outputs chosen from the following 4 possibilities:

No Output

X

X-D, X+D

X-D, X, X+D

Here D is a preprogrammed function of W.

The internal two-phase clock begins an output cycle by activating the READ INHIBIT signal to the appropriate stack. This is not done if a J chamber centroid has been received because the output will go to the J processor (discussed later). Next, if enabled by the W PROM, the results of the subtraction will be output to the appropriate stack, or to the J processing section. Then, simultaneously, the arithmetic unit adds the offset to the centroid, and the centroid itself is output if enabled by the PROM. Finally, the results of the addition is output if enabled. The last thing that happens, is the updating of the module status. That is, START bits and STOP bits are sampled. If at least one data word has been received from all three chambers, the START signal to the Track Finder (ECL 9/10) is activated. If a STOP bit has been received from each chamber, and the J processor is not still active, the START signal will be deactivated signalling the receipt of all data. The READ INHIBIT signal is removed during status update.

If a J chamber centroid was received, the subtraction occurs as before and the results are clocked into a counter in the J processor. The width, while being decoded by the WIDTH PROM,

is simultaneously decoded by two PROMs in the J processor. The outputs of these PROMs are clocked into a 16-bit shift register to be used as a control word. Also, Request To Send (RTS) is sent to the Track Finder J chamber hit array. Upon receipt of Clear To Send (CTS) from ECL 9/10 the rightmost bit in the control word is sampled. If it is set, the number contained in the counter is output to the hit array. RTS remains high, the control word is right-shifted, and the counter is incremented. The control bit is then sampled and the process repeats itself until 16 possible outputs have occurred. When all control bits have been sampled, RTS is lowered and the process ends.

The 16 J checks can be shortened by changing the number hardwired into the process counter IC-16 if it is desired to reduce the time required to process J data.

There are no CAMAC instructions.

PROM Programing

A. Width PROM (32x8 bits) (IC-54)

Input	Bits	Output	Bit
S Spread	0-3	D(offset)	0-3
J Middle Chmbr Flag	4	A outputs Z_o+D	4
		C outputs Z_o	5
		S outputs Z_o-D	6
		J Flags Mid. Ch	7

B. Mid Chamber (J) PROMs (Two PROMs, each 32x8 bits, IC-21,22)

These PROMs are only referenced if J=1 in the Width PROM, The input is the spread (S), Bits 0-3. The output is a 16-bit mini hit array (h). A one in a given bit of h will output a bit to the hit array in ECL 9/10 corresponding to the following coordinates:

B-PROM (IC-22)

X X X X X X X X

OUTPUT (Z-D+15)

A-PROM (IC-21)

X X X X X X X X

OUTPUT (Z-D)
OUTPUT (Z-D+1)
OUTPUT (Z-D+2)

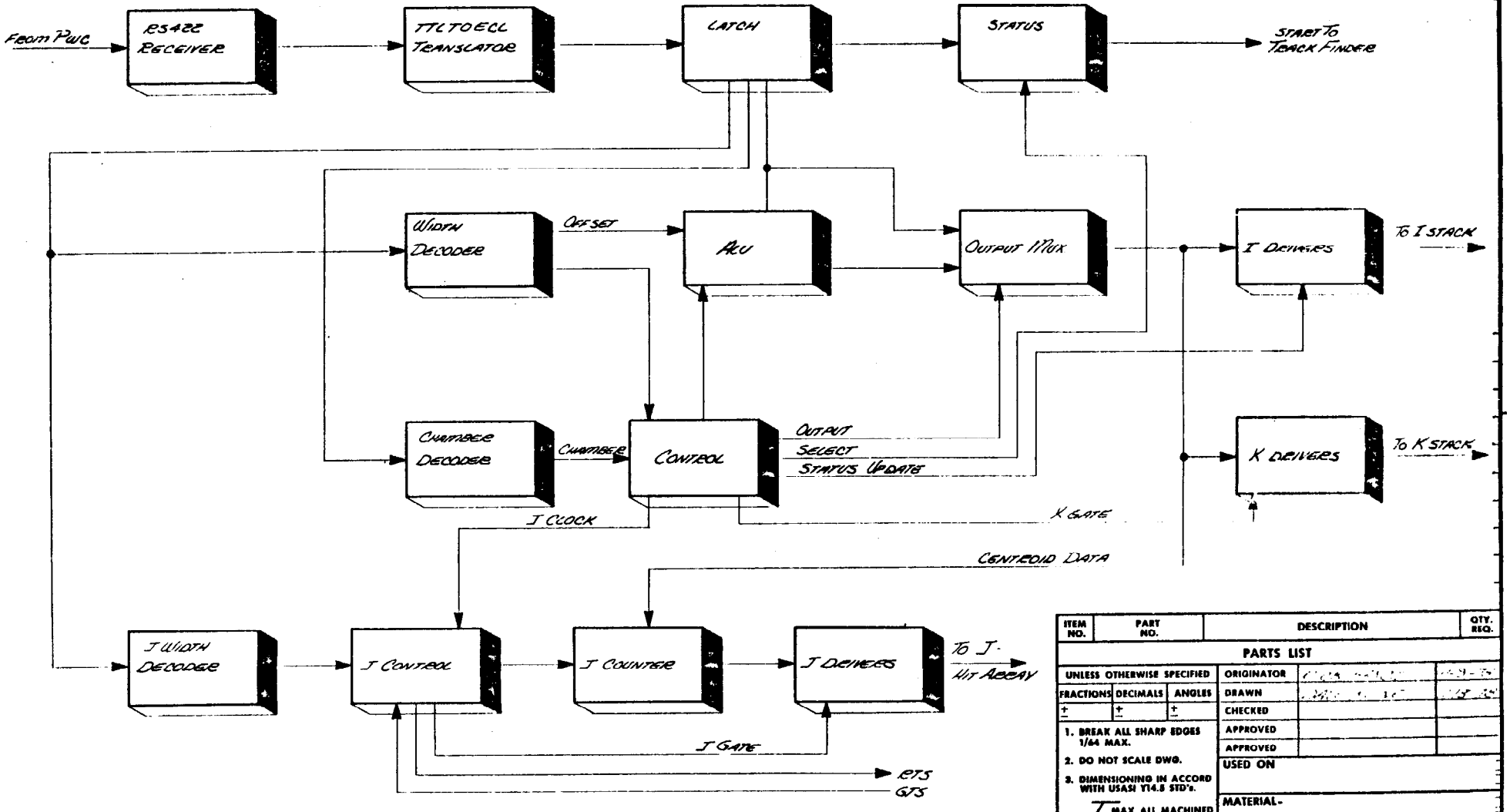
The tables on the following page show how the PROMs are programmed to produce the output addresses listed below (initial E516 testing application):

I or K Width	Output Addresses
0	none
1	none
2	X
3	X
4	X-1, X+1
5	X-2, X+2
6	X-3, X+3
7	X-4,X,X+4
8	X-5,X,X+5
9	X-6,X,X+6
10-15	none

J Width	Output Bits (1/2 wire units)
0	none
1	none
2	X-3,X-1,X+1,X+3
3	X-2,X,X+2
4	X-3,X-1,X+1,X+3
5	X-4,X-2,X,X+2,X+4
6	X-5,X-3,X-1,X+1,X+3,X+5
7	X-6,X-4,X-2,X,X+2,X+4,X+6
8	X-7,X-5,X-3,X-1,X+1,X+3,X+5,X+7
9	X-8,X-6,X-4,X-2,X,X+2,X+4,X+6,X+8
10-15	none

(Prepared by R. Hance, and T. Nash, 9/11/78)

REVISIONS			
SYM	DESCRIPTION	DRAWN APPD.	DATE DATE



ITEM NO.	PART NO.	DESCRIPTION	QTY. REQ.

PARTS LIST

UNLESS OTHERWISE SPECIFIED			ORIGINATOR	
FRACTIONS	DECIMALS	ANGLES	DRAWN	
±	±	±	CHECKED	
			APPROVED	
			APPROVED	

1. BREAK ALL SHARP EDGES 1/64 MAX.
2. DO NOT SCALE DWG.
3. DIMENSIONING IN ACCORD WITH USASI Y14.5 STD'S.

√ MAX. ALL MACHINED SURFACES

USED ON

MATERIAL -

NATIONAL ACCELERATOR LABORATORY
U.S. ATOMIC ENERGY COMMISSION

BEAM SYSTEMS
ECL-6
BLOCK DIAGRAM

SCALE	FILMED	DRAWING NUMBER	REV.

NING

ECL-6 PWC RECEIVER PROMS-PROGRAMMING MAP

WIDTH PROM

	WIDTH					CONTROL-OFFSET									
	J	W3	W2	W1	W0	J	S	C	A	4	3	2	1	OFFSET	OUTPUT
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NONE
	1	0	0	0	1	0	0	0	0	0	0	0	0	0	NONE
	1	0	0	1	0	0	0	1	0	0	0	0	0	0	X
	1	0	0	1	1	0	0	1	0	0	0	0	0	0	X
	1	0	1	0	0	0	1	0	1	0	0	1	0	2	X-2 X+2
	1	0	1	0	1	0	1	0	1	0	0	1	0	2	X-2 X+2
	1	0	1	1	0	0	1	0	1	0	0	1	1	3	X-3 X+3
Dark	1	0	1	1	1	0	1	0	1	0	1	0	0	4	X-4 X+4
	1	1	0	0	0	0	1	0	1	0	1	0	0	4	X-4 X+4
	1	1	0	0	1	0	1	1	1	0	1	1	0	6	X-6 X X+6
	1	1	0	1	0				0					0	NONE
	1	1	0	1	1				0					0	NONE
	1	1	1	0	0				0					0	NONE
	1	1	1	0	1				0					0	NONE
	1	1	1	1	0				0					0	NONE
	1	1	1	1	1				0					0	NONE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NONE
	0	0	0	0	1	0	0	0	0	0	0	0	0	0	NONE
	0	0	0	1	0	1	1	0	0	0	0	0	1	1	
	0	0	0	1	1	1	1	0	0	0	0	1	0	2	To
	0	0	1	0	0	1	1	0	0	0	0	1	1	3	
	0	0	1	0	1	1	1	0	0	0	1	0	0	4	J
J	0	0	1	1	0	1	1	0	0	0	1	0	1	5	
	0	0	1	1	1	1	1	0	0	0	1	1	0	6	PROCESSOR
	0	1	0	0	0	1	1	0	0	0	1	1	1	7	
	0	1	0	0	1	1	1	0	0	1	0	0	0	8	
	0	1	0	1	0				0					0	NONE
	0	1	0	1	1				0					0	NONE
	0	1	1	0	0				0					0	NONE
	0	1	1	0	1				0					0	NONE
	0	1	1	1	0				0					0	NONE
	0	1	1	1	1				0					0	NONE

J=RESULTS GO TO J PROCESSOR
S=OUTPUT X-OFFSET
C=OUTPUT X
A=OUTPUT X+OFFSET

ECL-6 PWC RECEIVER PROMS-PROGRAMMING MAP

J PROCESSOR CONTROL PROM

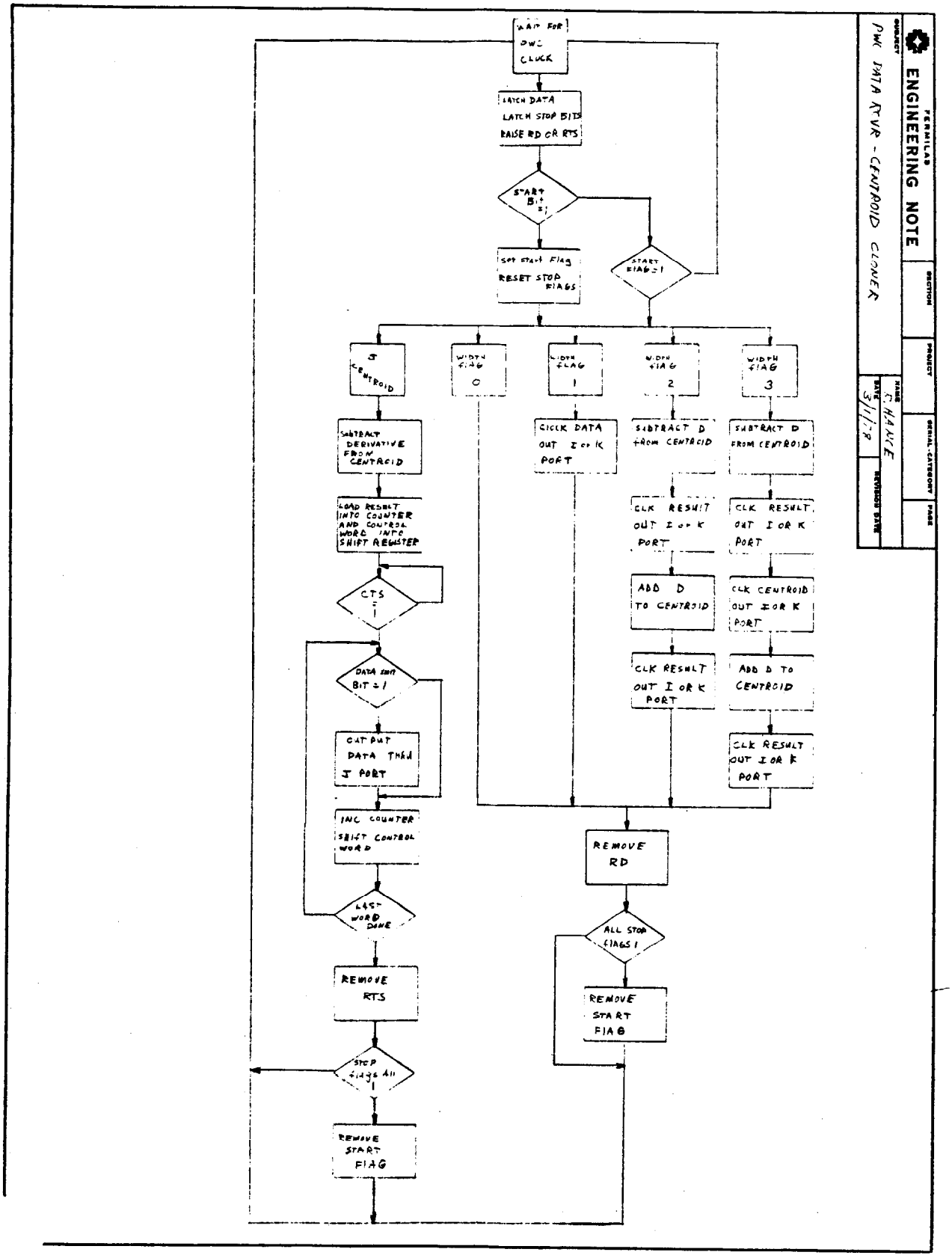
WIDTH X W3 W2 W1 W0 / A4 A3 A2 A1 A0	B PROM DATA 7 6 5 4 3 2 1 0	A PROM DATA 7 6 5 4 3 2 1 0
0 0 0 0 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
0 0 0 0 1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0
0 0 0 1 0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1 1
0 0 0 1 1	0 0 0 0 0 0 0 0	0 0 0 0 0 1 1 1
0 0 1 0 0	0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1
0 0 1 0 1	0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1
0 0 1 1 0	0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1
0 0 1 1 1	0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1
0 1 0 0 0	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1
0 1 0 0 1	0 0 0 0 0 0 0 1	1 1 1 1 1 1 1 1
0 1 0 1 0	0	0
0 1 0 1 1	0	0
0 1 1 0 0	0	0
0 1 1 0 1	0	0
0 1 1 1 0	0	0
0 1 1 1 1	0	0
1 0 0 0 0	0	0
* * * 1 1 1 1 1	UNUSED	UNUSED

A "1" IN DATA WILL OUTPUT A CENTROID:

B PROM
X X X X X X X X
└ OUTPUT (X-OFFSET)+15

A PROM
X X X X X X X X
└ OUTPUT (X-OFFSET)
└ OUTPUT (X-OFFSET)+1
└ OUTPUT (X-OFFSET)+2

1/2 WIRE BITS ARE NOT USED BY THE J PROCESSOR

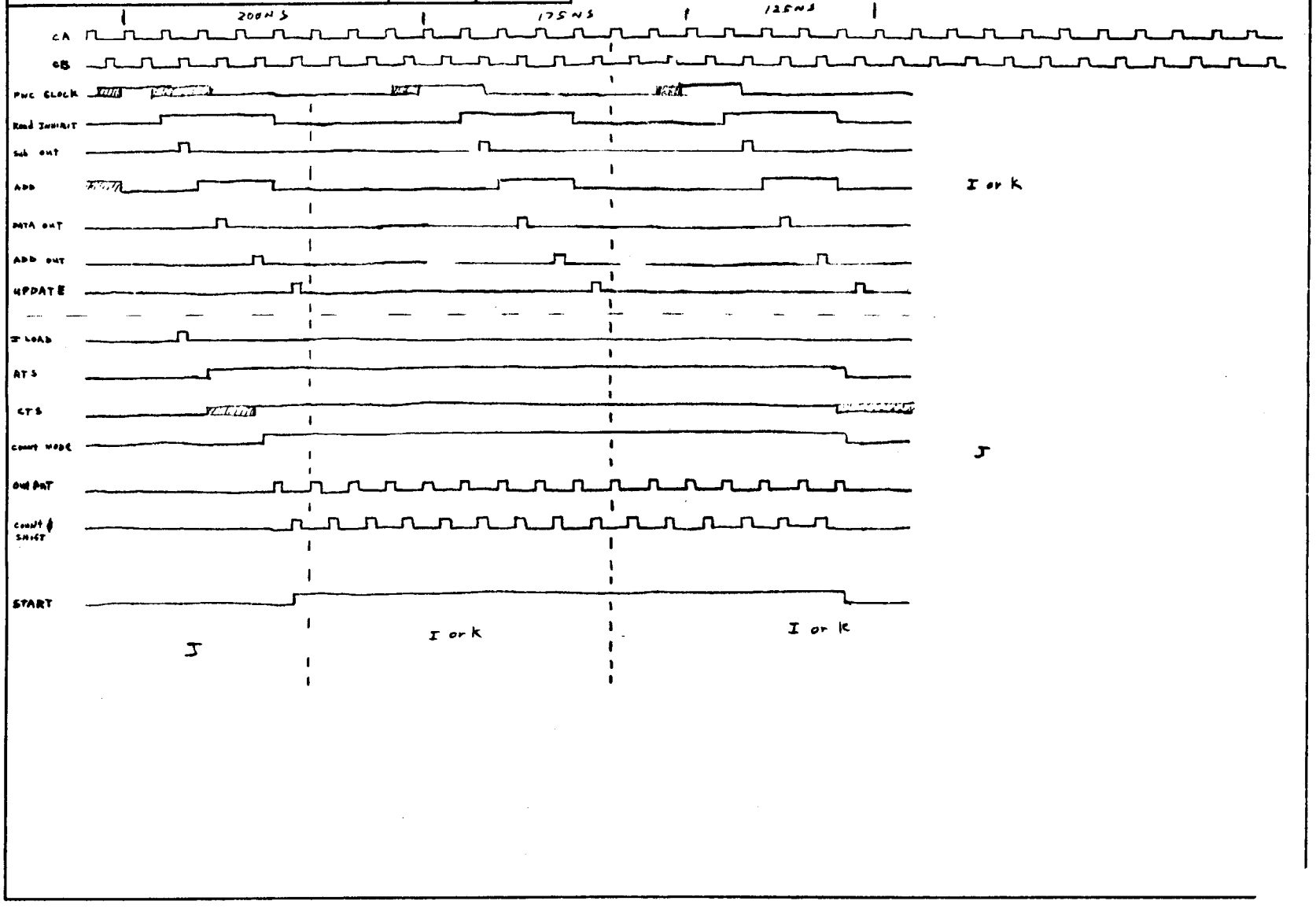

WAIT FOR DWC CLOCK
LATCH DATA
LATCH STOP BITS
RAISE RD OR RTS
START BIT = 1
SET START FLAG
RESET STOP FLAGS
START FLAG = 1
J CENTROID
WIDTH FLAG 0
WIDTH FLAG 1
WIDTH FLAG 2
WIDTH FLAG 3
SUBTRACT DERIVATIVE FROM CENTROID
CLOCK DATA OUT I or K PORT
SUBTRACT D FROM CENTROID
SUBTRACT D FROM CENTROID
LOAD RESULT INTO COUNTER AND CONTROL WORD INTO SHIFT REGISTER
CLK RESULT OUT I or K PORT
CLK RESULT OUT I OR K PORT
CTS = 1
ADD D TO CENTROID
CLK CENTROID OUT I OR K PORT
DATA BIT BIT = 1
CLK RESULT OUT I OR K PORT
ADD D TO CENTROID
OUTPUT DATA THRU J PORT
CLK RESULT OUT I OR K PORT
INC COUNTER SHIFT CONTROL WORD
REMOVE RD
LAST WORD DONE
ALL STOP FLAGS 1
REMOVE RTS
REMOVE START FLAG
STOP FLAGS ALL 1
REMOVE START FLAG
ENGINEERING NOTE
SUBJECT
PWC DATA RVR - CENTROID CLOCKER
NAME
C. HANKE
DATE
3/11/92

FERMILAB
ENGINEERING NOTE

SECTION | PROJECT | SERIAL-CATEGORY | PAGE

SUBJECT: COMPOSITE TIMING - CENTROID PROCESSOR

NAME | DATE | REVISION DATE



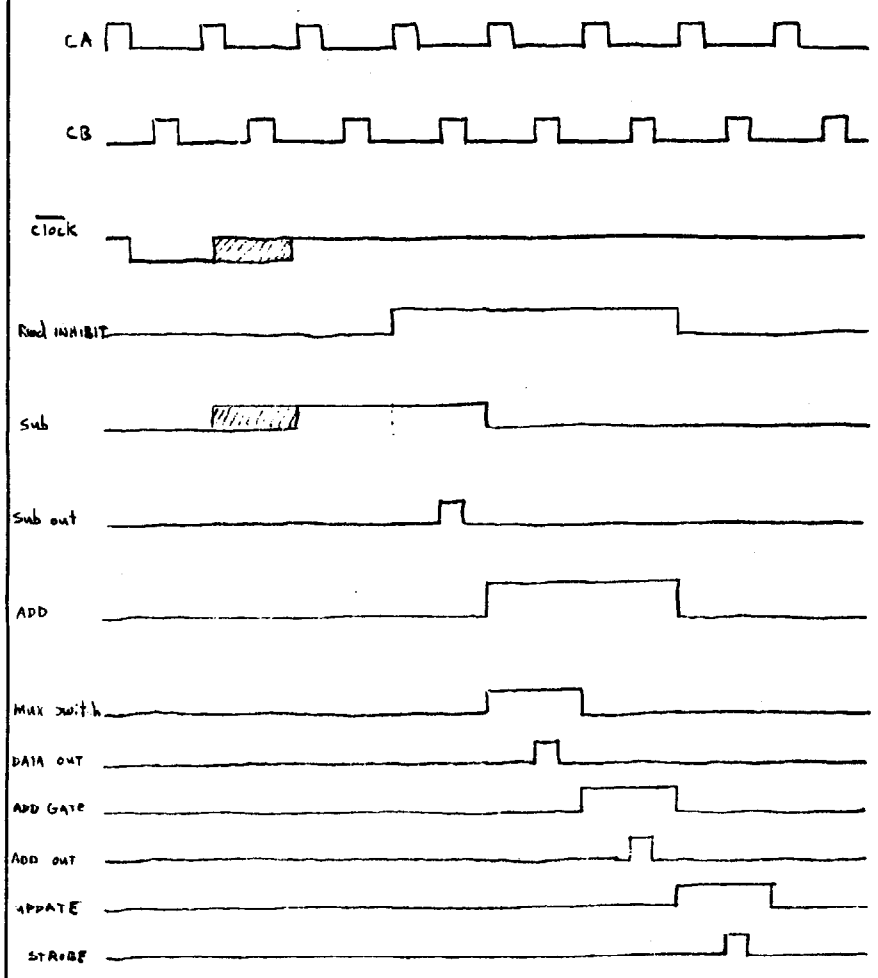
FERMILAB **ENGINEERING NOTE**

SUBJECT: PWC CENTROID PROCESSOR I & K CHAMBERS

NAME: R. HANCE

MAX CYCLE TIME WITHOUT OVERRUN = 135 NS
MIN CYCLE " " " = 112 NS

STACK WRITES OCCUR 25 NS APART



clock FROM PWC XMITTER

"CAPTURES" STACK DURING ACCESSING

STROBES (CENTROID - offSET) ResulT, If USED AS DETERMINED BY WIDTH DATA, INTO STACK

PERFORMS (CENTROID + OFFSET) CALCULATION

STROBES UNMODIFIED CENTROID, If USED, INTO STACK

STROBES (CENTROID + offSET) RESULT, If USED, INTO STACK

Lowers START LINE If ALL CENTROIDS FROM I & K CHAMBERS HAVE BEEN PROCESSED

START IS RAISED ON 1st "STROBE" COINCIDING WITH START BITS BEING RECEIVED from I, J, K

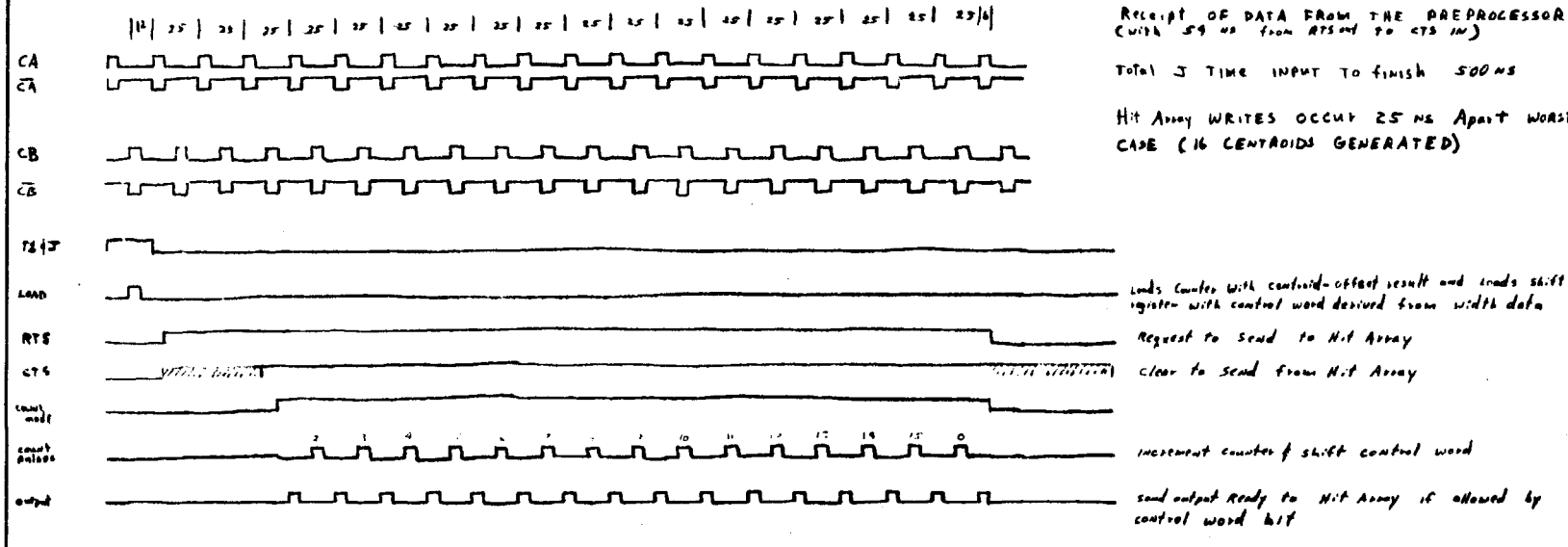
FERMILAB **ENGINEERING NOTE**

SECTION	PROJECT	SERIAL-CATEGORY	PAGE

SUBJECT: PWC CENTROID PROCESSOR – J CHAMBER

NAME: R. HANCE

DATE: | REVISION DATE:



J PROCESSOR CYCLE TIME 470 NS FROM Receipt OF DATA FROM THE PREPROCESSOR (WITH 59 NS from RTS out TO CTS IN)

Total J TIME INPUT TO finish 500 NS

Hit Array WRITES OCCUR 25 NS Apart WORST CASE (16 CENTROIDS GENERATED)

NOTES:

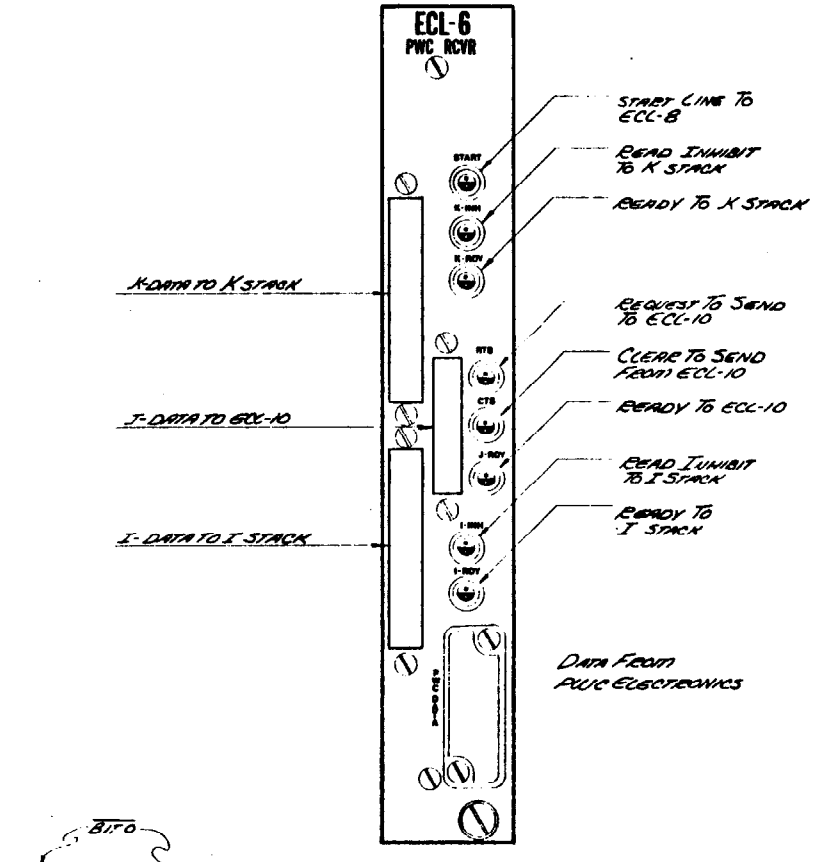
Total "J" Processing TIME DEPENDS TO AN EXTENT ON HOW FAST THE HIT ARRAY RETURNS CTS. MINIMUM PROCESSING TIME WOULD BE 500NS START TO FINISH – CTS CAN TAKE UP TO 31 NS IN THIS CASE.

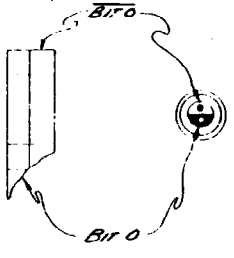
"I & K" CENTROIDS CAN BE Received AS Soon AS 150NS After receipt of A "J" CENTROID

FRONT

11-10101	20-10101	31-10101	42-10101	51-10101	62-26C532
10-10101	19-10101	30-10101	41-10101	50-26C5-32	61-26C532
9-10173	18-10136	29-10139	40-10114	49-26C5-32	60-26C532
8-10173	17-10173	28-10136	39-	48-10124	59-10124
7-10181	27-10181	38-		58-10124	
6-10181	26-10104	37-10103		57-10124	
5-10195	16-10136	25-10102	36-10104	47-10124	56-10176
4-	15-10141	24-10104	35-10104	46-10176	55-10176
3-10104	14-10141	23-10131	34-10102	45-10135	54-10139
2-10131	13-10141	22-10139	33-10141	44-10135	53-10171
1-10102	12-10141	21-10139	32-10131	43-10135	52-10135

REVISIONS			
SYM	DESCRIPTION	DRAWN / APPD.	DATE / DATE





ITEM NO.	PART NO.	DESCRIPTION	QTY. REQ.
PARTS LIST			

UNLESS OTHERWISE SPECIFIED			ORIGINATOR
FRACTIONS ±	DECIMALS ±	ANGLES ±	DRAWN
			CHECKED
1. BREAK ALL SHARP EDGES 1/64 MAX.			APPROVED
2. DO NOT SCALE DWG.			APPROVED
3. DIMENSIONING IN ACCORD WITH USASI Y14.5 STD's.			USED ON
√ MAX. ALL MACHINED SURFACES			MATERIAL-

NATIONAL ACCELERATOR LABORATORY
U.S. ATOMIC ENERGY COMMISSION

BEAM SYSTEMS
ECC-6
FRONT PANEL LAYOUT

SCALE	FILMED	DRAWING NUMBER	REV.

FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	Exp. 516	TM-0821	94

SUBJECT

DOCUMENTATION OF: ECL-6

NAME: H. James Krebs

DATE	REVISION DATE
6-22-78	

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-ED-104393
FRONT PANEL MACHING DRAWING	0880-MC-104453
FRONT PANEL ASSEMBLY	0880-MC-104454
FRONT PANEL ARTWORK	
MODULE FINAL ASSEMBLY	
P.C. CARD COMPONENT ASSEMBLY	
P.C. CARD DRILL DRAWING	
P.C. CARD PARTS LIST	0880-MA-104455
P.C. CARD MASTER ARTWORK	
BOARD OUTLINE	

ECL/CAMAC MODULE ECL-7

PWC Data Test Transmitter

(Limited Purpose Test Module -

Wire Wrapped - Double Width)

General Description

This module provides a means to send simulated proportional wire chamber (PWC) data to the trigger processor for testing.

The module consists of a 19-bit by 64 word FIFO memory, ECL/CAMAC logic for loading and reading the memory, and control circuits for outputting the contents of memory to the trigger processor at rates of up to 10 MHZ. Data is transmitted at E.I.A. standard RS422 levels, and consists of 19-bits of parallel data and a clock.

Data format to simulate a PWC is as follows:

18	17	16	15	14 — 11	10 — 0
Start	Stop	Chamber		Cluster Width	Cluster Centroid Address

Msb

Output is via a front panel mounted Amp 54 pin high density rectangular connector. Pin out is given on the schematic diagram.

Programming

F9 A0 Reset internal index pointer to zero.

F16 AX Write cluster width and centroid address to current index location, and increment index pointer, R/W bits 1 thru 4 are used.

F25 A0 Trigger output cycle. At this time, the current index value is latched to be used as a word count. Then, the module proceeds to output data and clock starting at index location 0 and continuing until the index reaches the latched word count. Repeated triggers will give repeated transfers.

F0 AX Read cluster width and centroid address from current index location, and increment index pointer. Data format is the same as for F16 AX.

F1 AX Read start, stop, and chamber data from current index location, and increment index pointer. Data format is the same as for F17 AX.

F4 A0 Read current index value. R/W 1 thru R/W 6 are used.

The module returns X for all commands and Q for all executable commands. The reset command is always executable but the others will not return Q if the module is in the process of outputting data.

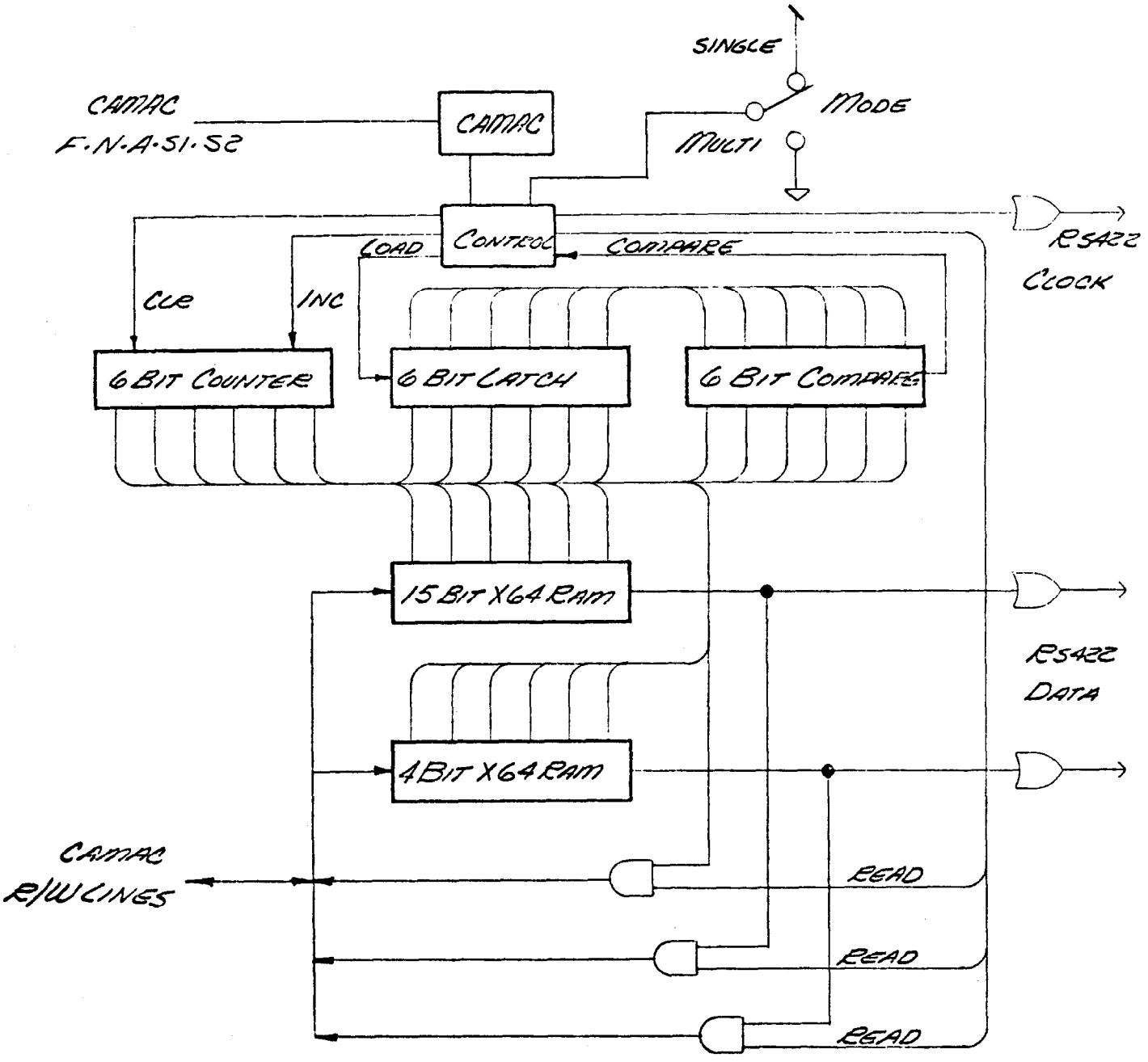
Front Panel

The front panel contains the following:

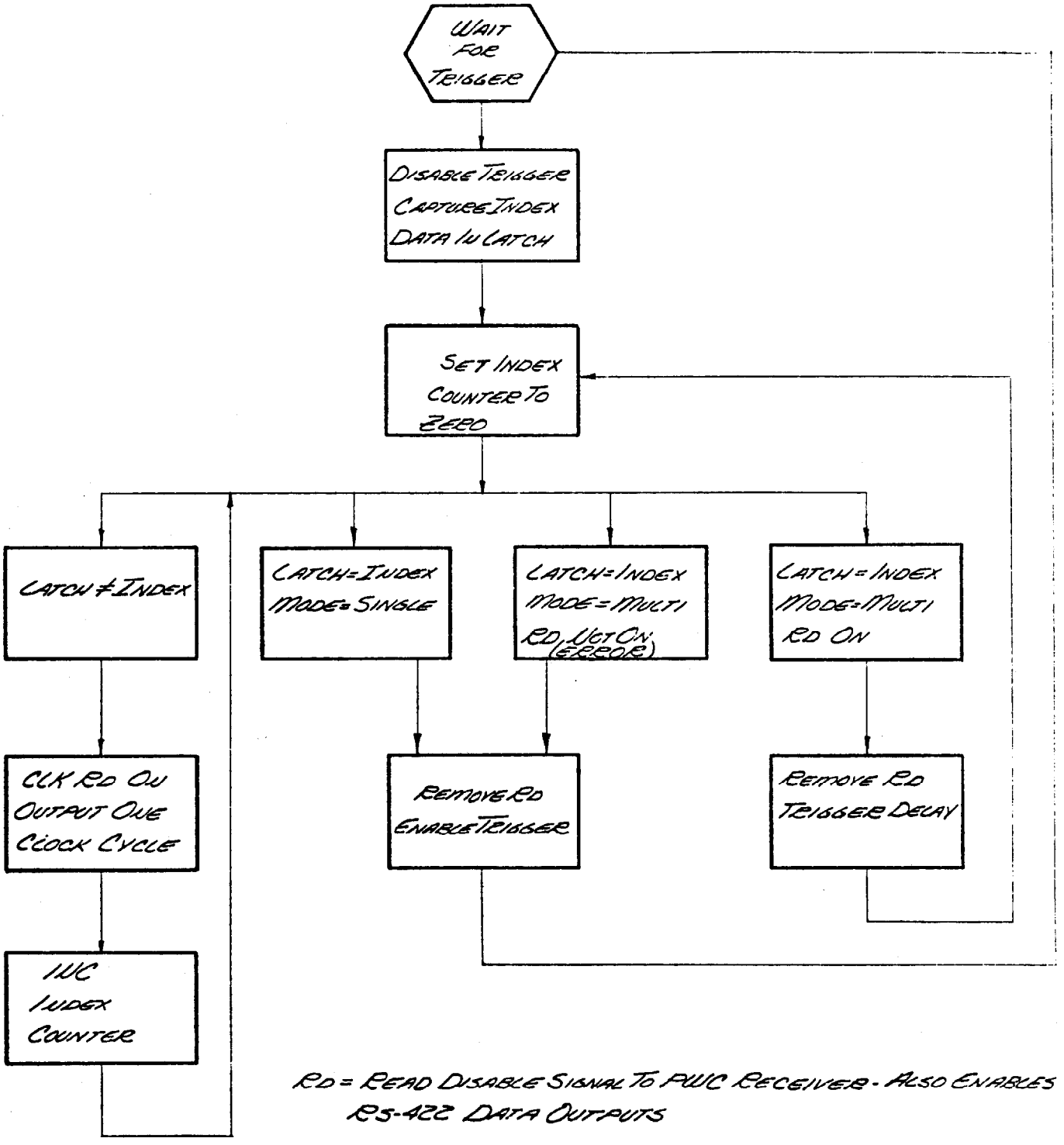
"N" Test Point	An ECL logic one level indicates the module is being accessed by CAMAC.
"Xmit Sync"	An ECL logic zero to one transition signals the beginning of a transfer of all the data in the FIFO.
"Clock Out"	ECL level data clock, active only during data transmission.
Data Connector	54-pin high density rectangular connector for interfacing RS-422 data and clock to the trigger processor.
Mode Switch	A lock-lever switch is used to place the module into the Multi or Single mode of operation. In the multi-mode, the module does not stop after a data transmission. It waits a short time then retriggers itself. This mode is intended for maintenance purposes.

(Prepared by R. Hance, 3/7/78)

PWC DATA TRANSMITTER

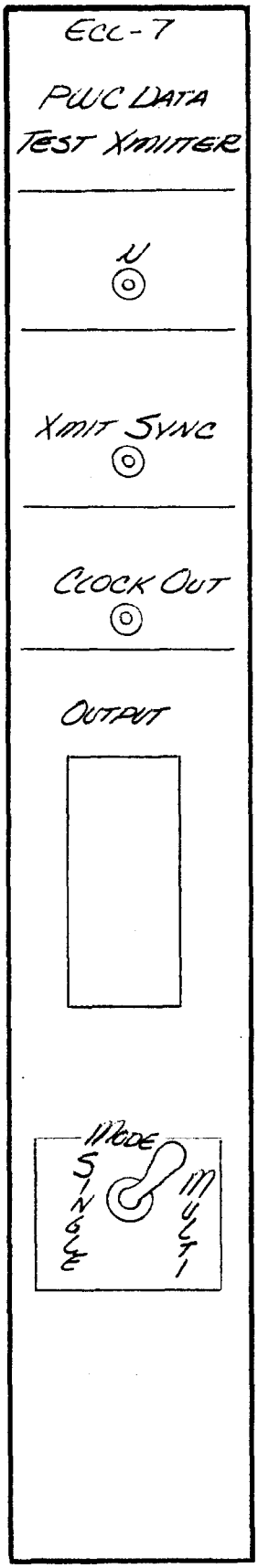


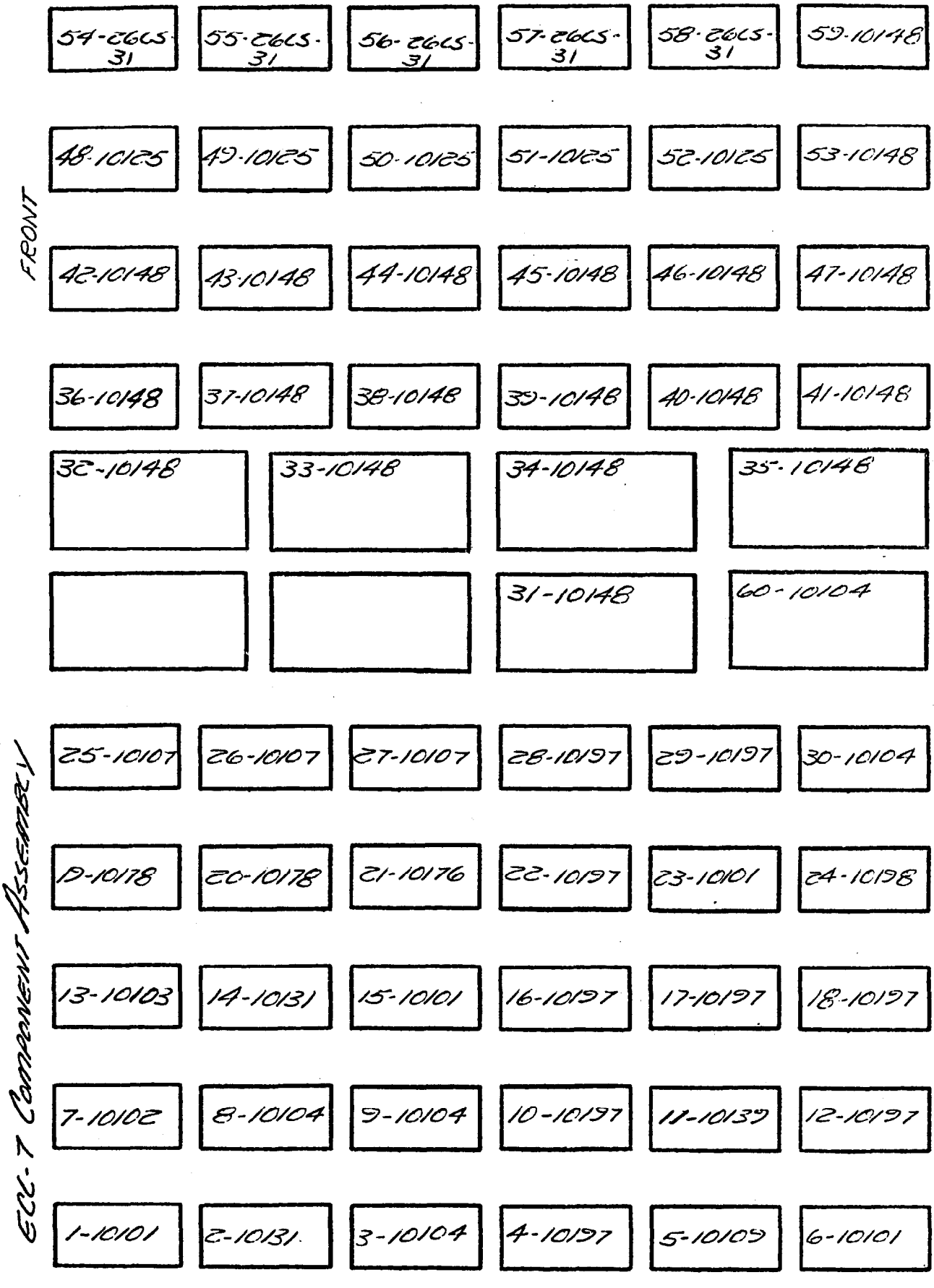
PWC Data Simulator Output Controller



RD = Read Disable Signal To PWC Receiver - Also Enables RS-422 Data Outputs

ECL-7 PWC TEST TRANSMITTER




54-2665-31
55-2665-31
56-2665-31
57-2665-31
58-2665-31
59-10148
48-10125
49-10125
50-10125
51-10125
52-10125
53-10148
FRONT
42-10148
43-10148
44-10148
45-10148
46-10148
47-10148
36-10148
37-10148
38-10148
39-10148
40-10148
41-10148
32-10148
33-10148
34-10148
35-10148
31-10148
60-10104
REAR
25-10107
26-10107
27-10107
28-10197
29-10197
30-10104
19-10178
20-10178
21-10176
22-10197
23-10101
24-10198
13-10103
14-10131
15-10101
16-10197
17-10197
18-10197
7-10102
8-10104
9-10104
10-10197
11-10137
12-10197
1-10101
2-10131
3-10104
4-10197
5-10109
6-10101
ECL-1 Component Assembly

FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	Exp. 516	TM-0821	102

SUBJECT

DOCUMENTATION OF:
ECL-7

NAME
H. James Krebs

DATE
6-23-78

REVISION DATE

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-ED-104321
FRONT PANEL MACHING DRAWING	0880-MC-104456
FRONT PANEL ASSEMBLY	0880-MC-104457
FRONT PANEL ARTWORK	
MODULE FINAL ASSEMBLY	
P.C. CARD COMPONENT ASSEMBLY	
P.C. CARD DRILL DRAWING	
P.C. CARD PARTS LIST	0880-MA-104458
P.C. CARD MASTER ARTWORK	
BOARD OUTLINE	

ECL/CAMAC ECL-8

Double Index Do Loop Indexer

(General Purpose Module - Wire Wrapped - Double Width)

General Description

This module acts as a controller that cycles through all values of 2 indices (I, K) much like a Fortran DO loop except that the upper limits may increase while the loop is in operation. Each pair of I > 0, K > 0 (or KMIN (I) as explained below) up to the upper limits at the end of data transmission is presented on the I, K outputs once and only once. Upper limits at any moment are flagged externally by signals at the ITH or KTH inputs to this module. The module is able to control the random read of data from two stacks (for track finding, for example) while the stacks are still being filled with data (from MWPC readout, for example). A description of the use of this module in the track finding subsystem may be found in the ECL 9/10 section.

Inputs		Bits
ITH	(I Too High-Set if I > IMAX(I))	1
KTL	(K Too Low-Set if K < KMIN(I)) used to avoid wasteing time on steep backward tracks, for example)	1
KTH	(K Too High-Set if K > KMAX(I))	1
CONT	(Request next I, K used if	1
	$\overline{ITH}.\overline{KTL}.\overline{KTH}$	1
START	(On while data is being transmitted to stack. Leading edge when at least I=1 and K=1 are wanted. Trailing edge indicates all data is in and controller should perform one last pass through unused indices	1
RESET	(Reset all indices, counters, etc. to initial conditions	1

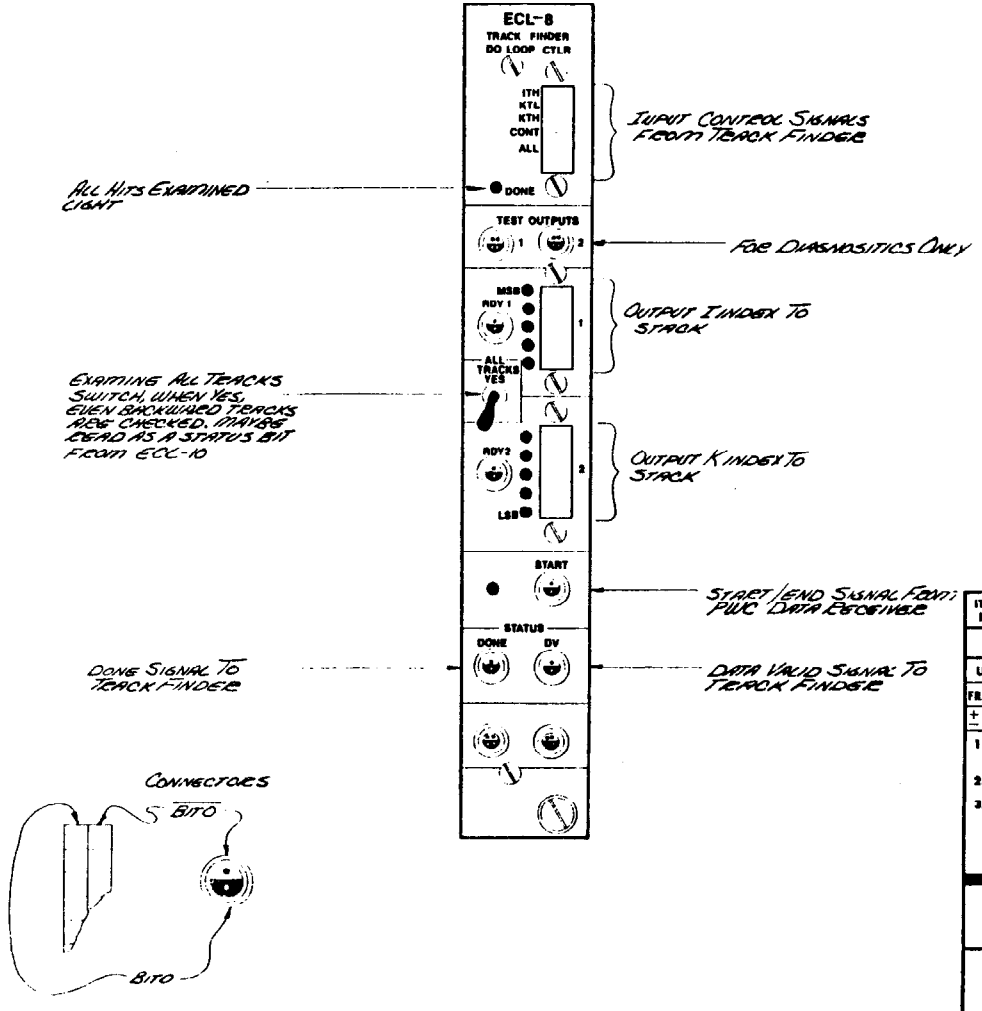
Output		Bits
ALL (Set by front panel switch if KTL to be ignored)		1
I (Index 1)		5
K (Index 2)		5
RDY1 (IRDY)	I and K Ready	1
RDY2 (KRDY)		
RDY3 (VALID)		1
DONE (all index completed)		1
TEST OUTPUTS 1		1
" " 2		1

(Comes on when I, K come on. Goes off when ITH or KTL or KTH or CONT is received)

There are no CAMAC commands for this module. All testing done by monitoring and control from other modules.

REVISIONS			
SYM	DESCRIPTION	DRAWN / APPD.	DATE / DATE

105



ITEM NO.	PART NO.	DESCRIPTION	QTY. REQ.

PARTS LIST

UNLESS OTHERWISE SPECIFIED			ORIGINATOR	
FRACTIONS	DECIMALS	ANGLES	DRAWN	
±	±	±	CHECKED	
			APPROVED	
			APPROVED	

1. BREAK ALL SHARP EDGES 1/64 MAX.
2. DO NOT SCALE DWG.
3. DIMENSIONING IN ACCORD WITH USASI Y14.5 STD's.

√ MAX. ALL MACHINED SURFACES

USED ON

MATERIAL-

NATIONAL ACCELERATOR LABORATORY
U.S. ATOMIC ENERGY COMMISSION

BEAM SYSTEMS
ECL-8
FRONT PANEL LAYOUT

SCALE	FILMED	DRAWING NUMBER	REV.
FULL			

The Basic Algorithm

At the beginning of each cycle the module examines the input control bits (ITH, KTH, CONT, KTL, etc.). Using backing registers it quickly outputs new indices. Basically, the algorithm followed is this:

1. If neither ITH or KTH is true but CONT is received, then the new I is equal to the old I and K is incremented.
2. If KTH is true but ITH is not, I is incremented and K is set back, for an I that has never been tried before, K is SET TO ZERO: FOR AN I that has already been partially examined. K is set to the value of K that last caused KTH to be set. No I, K pair will be transmitted twice.
3. If ITH is true, I is set back to zero and K is set back as explained below. If all data was in the last time I was set back, then the pass thru all the indices just performed is the last required, and ITH will cause a DONE signal. No more indices will be sent.

ECL-8 Structure and Operation

RESET clears a few registers and sets a flip-flop called INITF. INITF forces an ITH mode, so indexing begins at I=0 and K=0. INITF is immediately reset and remains reset until the next event is to be taken.

The indexer keeps track of what K values it has already tried for each I. A 5-bit by 32 word memory stores the next

value of K to try for a given value of I. The table is indexed by I. Whenever I is to be changed due to KTH, the current (failed) value of K is saved in KSTRT(I). I is incremented, and K is set to KSTRT(I) for the new I. This implies that all KSTRT(I) must be zero initially. There is no master clear, so another register called IMIN is used. It contains the first value of I that has not yet been used. Using an I means that something has been stored in KSTRT(I). If an unused I is attained (initially all I are unused) then 0 is substituted for KSTRT(I) in loading K. If KSTRT(I) is loaded for I greater than IMIN, then IMIN is incremented to the new value of I.

In processing all the K associated with a given I, a value of K may be found to be (tracks going backward, for example). In this case, KTL will be returned. If a given K is too low for this I, then it is assumed too low for the next ones as well. A KMIN register is provided which is set to 0 whenever I is set to 0, and is set to K+1 whenever KTL is returned. When I is incremented, K is normally set to 0 (I greater than or equal to IMIN), or KSTRT(I) (I less than IMIN). If KMIN is greater than whichever of these would normally be loaded into K, then it is used instead.

Behind each output register (I and K) are backing registers. These registers may be quickly loaded into the registers they back, and together contain all possible results of the next request for indices.

Considering the three basic modes:

CONT I stays the same. Increment K

KTH I incremented, K set back to 0 or KMIN or KSTRT(I)

ITH I set to 0, K set back to 0 or KSTRT(0)

I has only one backing register which holds I+1; it is called IP1. K has three backing registers, one for each basic mode. One holds K+1, another holds KSTRT(IP1) or KMIN or 0, and a third holds KSTRT(0) or 0. KSTRT(0) is a special register called KST0.

When a request for new indices is received (ITH, KTH, KTL or CONT), logic in this module quickly (<20NS) decides which index alteration scheme is needed and the appropriate backing registers are loaded into the output registers. Then, DATA VALID is brought high, indicating that I and K are ready to use. While external modules use this I and K, this module is restoring its backing registers. This is done in parallel. To do it quickly, certain auxilary registers are used. For example, ILAG is almost always equal to I but at a certain point lags a few NS behind it. The backing registers will be ready for use before the next request for indices. Related functions such as handling KSTRT, LASTF and INITF are also done after I and K are valid and the external modules are working.

When START goes low, the module is forced into the ITH mode to make a final pass with all unused data in the stacks. A flip flop called LASTF is set when ITH mode is forced in this way; it prevents ITH from being forced again and again. DONE is set when ITH arrives (end of final pass).

(Prepared by S. Bracker, R. Hance, T. Nash - 10/1/78)

FERMILAB **ENGINEERING NOTE**

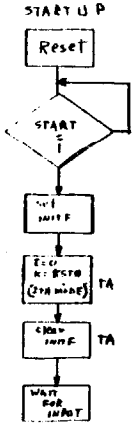
SUBJECT: ECL-8 TIMING STATES

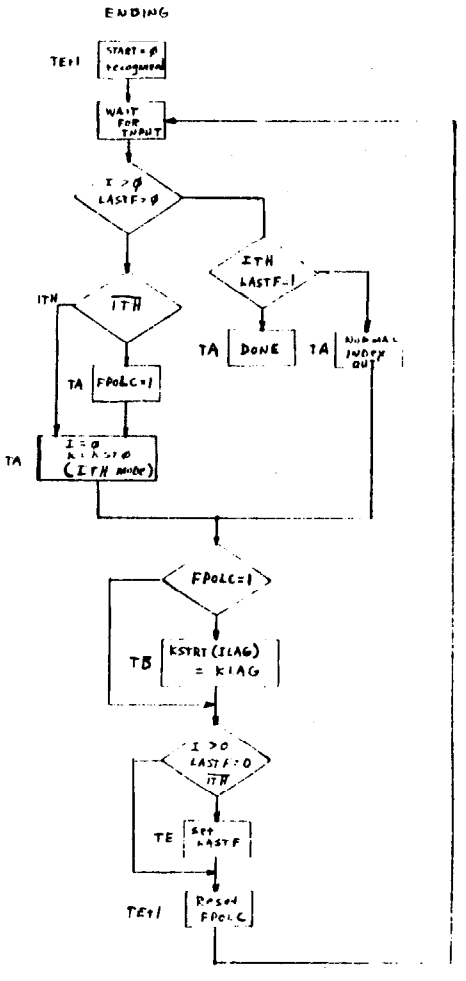
DATE: 6/8/78

	TA	TB	TE	TE+1
CONT DV=0	I=I K=KP1 KP1 = INPUT of k	DATA VALID = TRUE	KP1 = KP1+1 KLAG = k	ILAG = I
KTH DV=0	I=IP1 K {KMIN* if IMIN<IP1 {KSTRT(IP1) ϕ if KMIN* (whichever is larger) if IP1<IMIN* IP1 = INPUT of I KP1 = INPUT of k KTHF=1	KSTRT(ILAG)= KLAG DATA VALID = TRUE	IP1 = IP1+1 KP1 = KP1+1 KLAG = K KSTϕ = KLAG IF ILAG=ϕ	IMIN=IMIN+1 IF IMIN=ILAG ILAG = I KTHF = 0
KTL DV=0	I=I K=KP1 KMIN = KP1 KP1 = INPUT of K	DATA VALID = TRUE	KP1 = KP1+1 KLAG = K	ILAG = I
ITH OR ITH MODE DV=0	I=ϕ K=KSTϕ KMIN = ϕ IP1 = INPUT of I KP1 = INPUT of K KLAG = KLAG+1 IF $\overline{ITH} \cdot \overline{KTH}$	KSTRT(ILAG)= KLAG if (ITH·KTH)+FPOLC DATA VALID = TRUE	IP1 = IP1+1 KP1 = KP1+1 KLAG = K	ILAG = I

* KMIN = ϕ if all tracks are allowed
ϕ KSTRT (IP1) if all tracks are allowed

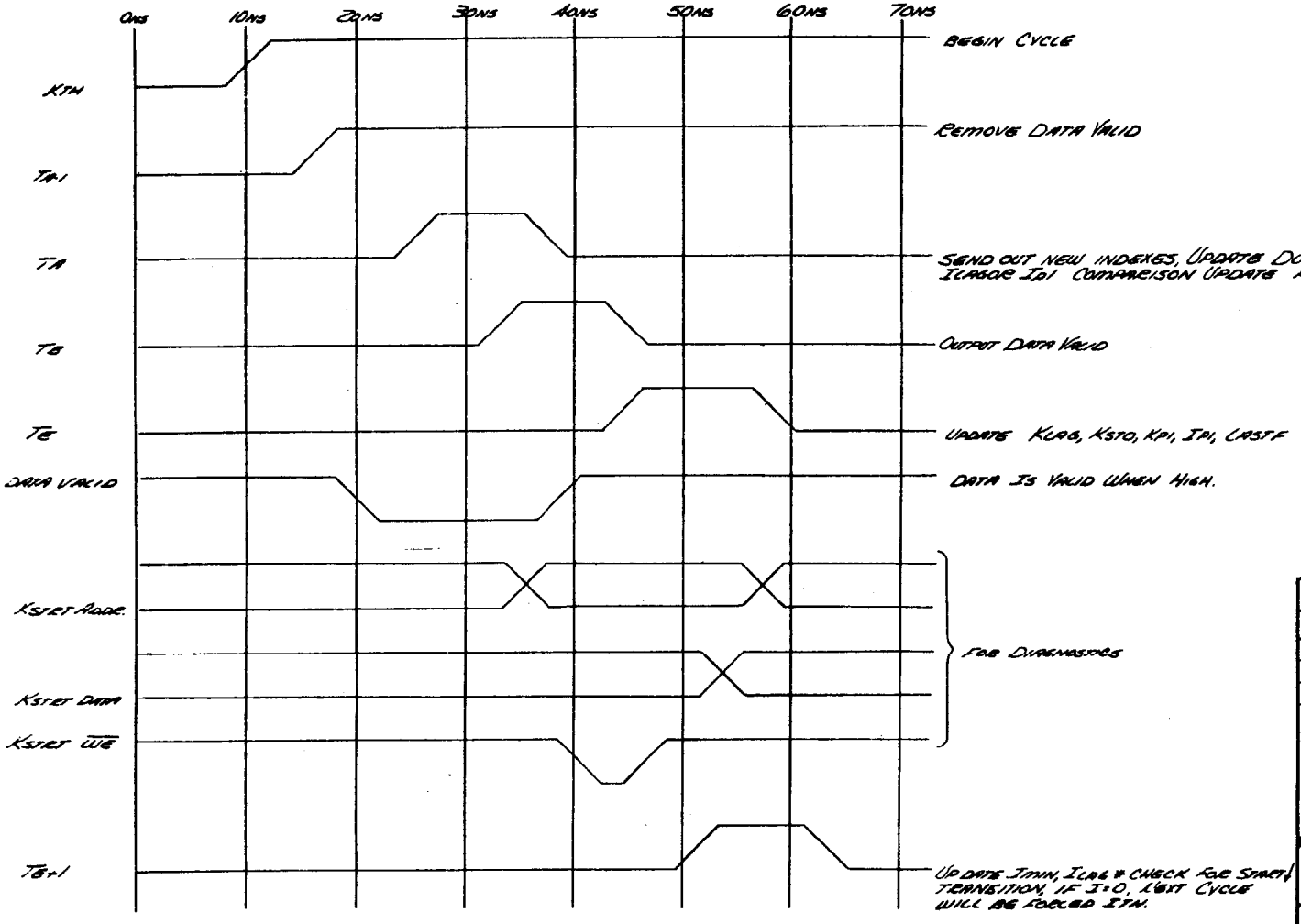
DV = DATA VALID
DV = ϕ at TA-1





NOTES:
Master Reset Resets: ILAG, IMIN, KLAG, KSTϕ, KTHF, DV, DONE, ALLF, LASTF
IMIN = MIN I FOR WHICH KSTRT(I) IS INVALID
KMIN = MIN K FOR THIS PASS THRU
IP1 = Normally I+1
ILAG = Normally I
KP1 = Normally K+1
KLAG = Normally K
KSTRT(0,31) = Lowest k which HASN'T Been Paired WITH GIVEN I
KSTϕ = KSTRT(ϕ)
INITF = SET IF UNIT INITIAL STATE LASTF = SET IF WITHIN FINAL PASS

REVISIONS			
SYM	DESCRIPTION	DRAWN / APPD.	DATE / DATE



ITEM NO.	PART NO.	DESCRIPTION	QTY. REQ.

PARTS LIST

UNLESS OTHERWISE SPECIFIED			ORIGINATOR	[illegible]	[illegible]
FRACTIONS	DECIMALS	ANGLES	DRAWN	D. KLINE	11-27-78
±	±	±	CHECKED		
1. BREAK ALL SHARP EDGES 1/64 MAX.			APPROVED		
2. DO NOT SCALE DWG.			APPROVED		
3. DIMENSIONING IN ACCORD WITH USASI Y14.5 STD's.			USED ON		
√ MAX. ALL MACHINED SURFACES			MATERIAL -		

NATIONAL ACCELERATOR LABORATORY
U.S. ATOMIC ENERGY COMMISSION

BEAM SYSTEMS
ECL-8
TIMING DIAGRAM

SCALE	PLATED	DRAWING NUMBER	REV.

FRONT

9-10114	16-10101	27-10101	36-10101		50-10114
8-10109		26-10101	35-10101	44-10109	49-10104
7-10104	16-10186	25-10186	34-10166	43-10109	48-10131
6-10131	15-10166	24-10145	33-10131	42-10195	47-10104
6A-10016	15A-10104	33A-10016	42A-10104		
5A-10016	14A-10109	32A-10105	46-10103		
5-10136	14-10197	23-10145	32-10158	41-10131	46-10136
4-10197	13-10174	22-10145	31-10158	40-10102	52-10103
3-10109	12-10174	21-10145	30-10195	39-10131	51-10131
2-10186	11-10174	20-ECC DM-45	29-10103	38-10109	X-10110
1-10186	10-10186	19-10104	28-10104	37-10131	

FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	Exp. 516	TM-0821	112

SUBJECT

DOCUMENTATION OF: ECL-8

NAME: H. James Krebs

DATE: 6-23-78

REVISION DATE:

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-ED-104322
FRONT PANEL MACHING DRAWING	0880-MC-104323
FRONT PANEL ASSEMBLY	0880-MC-104459
FRONT PANEL ARTWORK	
MODULE FINAL ASSEMBLY	
P.C. CARD COMPONENT ASSEMBLY	
P.C. CARD DRILL DRAWING	
P.C. CARD PARTS LIST	0880-MA-104460
P.C. CARD MASTER ARTWORK	
BOARD OUTLINE	

ECL/CAMAC MODULES ECL 9/10 TRACK FINDER

General Description of Track Finder Subsystem

Modules ECL 9-10 are designed to find straight line segments from 3 evenly spaced wire chambers, Z_I^{in}, Z_J^{mid}, Z_K^{out} (called PI, PJ, PK on the modules) which may be planar or concentric. By a fortuitous coincidence the system can be used without change to correlate hits in U, V, X wire chamber systems, where U and V refer to coordinate axis typically $\pm 20^{o}$ from X. In this case PI → U, PK → V, PJ → X, and in the following α → Y, etc. The Track Finder Subsystem is shown in the figure on the next page. The centroid address and widths of groups of wires which have been hit during the current event arrive at a PWC data receiver/ centroid processor (ECL-6). The PWC data receiver processes the centroid/width data, sorts it according to which chamber it came from, and creates hit information for the trigger processor. The PWC data receiver sends the I and K hits to stack modules where they are recorded in ascending order starting at 0 and holding the hit positions. The middle chamber (J) has its hits sent to a hit array in the Track Finder module ECL-10. These hits are indexed by position and hold a hit reference number meaningful to the Track Finder hardware. The Do Loop Controller (ECL 8-DLC) selects indices I and K and presents them as Random Read Addresses to two Stacks (ECL 4) containing Z_I^{in}

and Z_K^{out} which are then presented to this module. This module then calculates

$$PZ^{mid} = (Z_I^{in} + Z_K^{out})/2 = (PI + PK)/2 = PPJ$$

which is the predicted (projected) location in the middle chamber if this I, K corresponds to a track. As middle chamber (Z_J^{mid}) data is received it is used as a 10-bit address to a 4 x 768 bit RAM called the hit array $(H(Z_J^{mid}))$. This location is loaded with $H(Z_J^{mid}) = I_{ev}$, a 4-bit number (never 0000) that increments on each event and acts as an event identifier. After the projected mid-chamber position (PZ_J^{mid}) is calculated it is used to address the hit array. If $H(PZ^{mid}_J) = I_{ev}$ (for the present event), a track is found and the quantities

$$\alpha = Z_K^{out} - Z_I^{in} \quad \text{(the track slope)}$$

$$S\alpha = \begin{matrix} 1 & \alpha \geq 0 \\ 0 & \alpha \leq 0 \end{matrix}$$

$$V = \frac{3Z_I^{in} - Z_K^{out}}{Z} + OFF \quad \text{(track coordinate at one chamber sspacing unit inside inner chamber.)}$$

OFF is an alignment constant settable via onboard switches which must be set so $V \geq 0$ for good tracks. These quantities are computed simultaneously with PZ^{mid} and are available as soon as

the track decision has been made. If V < 0 the track is vetoed. The PWC Data Receiver (ECL6) can be programmed to load more than one coordinate into the hit array. This way, it is possible to loosen the track criterion to correspond to chamber resolution.

Data is being received by H(Z_J^{mid}) and the Z_I^{in}, Z_K^{out} stacks simultaneously with the track processing operations described above. The chamber data must be loaded into the stacks and hit array in an ordered way (upstream first, downstream last, for example). If PZ^{mid} > max (Z_J^{mid}) that has been received then KTH (K too high) is set to 1. If the Do Loop Indexer has attempted to index either stack beyond data received the stack will raise its DE level. This is received by this module at the Z^{in} Exh or Z^{out} Exh inputs and ITH (I too high) or KTH will be raised, as appropriate. These signals are used by the Indexer to determine the next indices. In addition if the ALL TRACKS input is set off (coming from the Indexer module) KTL (K too low) will be set if $\alpha < \alpha_{min}$, a parameter which may be set via on board switches. (If $\alpha < \alpha_{min}$ and a track has been found it will not be considered a track.) If a track is found or, if not found, and none of the KTH, KTL, ITH conditions exist, then CONT (continue) is set to instruct the Indexer to proceed.

The reason the hit array is 4 bits wide (instead of 1) is that large fast RAMs have no general clear. Thus to clear out

the hit array completely would take 768 loads, Even at 15 nsec each this would take over 10 μsec and cause an unacceptable dead time. Instead only 1/15 of the array is cleared after each event (starting on the Master Reset (MR), ABORT, or DONE input signals). Since there are 15 event identifiers (I_{ev}) all locations of the array with I_{ev} from the last time a given I_{ev} was used will have been cleared before the same I_{ev} is used again.

ECL 9/10 Time Estimates (from Data Valid (DV) signal)

Z^{in} Exh or Z^{out} Exh	ITH or KTH	16 nsec
KTH		44
KTL		53
CONT (no track)		58
CONT, TRACK RDY		63

On the following pages the two modules ECL9 and ECL10 are described individually in further detail.

General Description of ECL-9 Track Finder-1

This double wide ECL/CAMAC module is a special purpose module used in conjunction with ECL-10, Track Finder-2. This module calculates the projected location in the middle chamber (PPJ) which is used to address the hit array on ECL-10.

PPJ=(PI+PK)/2

PI is the inner chamber address and PK is the outer chamber address. ECL-9 is connected to ECL-10 via 34 pin flat ribbon cable connected between boards.

The module simultaneously calculates the track slope ($M\alpha$), the sign of the slope ($S\alpha$), and the offset vertex (OFV).

$$M\alpha = PK - PI$$

$$S\alpha = 1 \text{ IF } \alpha \geq 0,\ 0 \text{ IF } \alpha < 0$$

$$OFV = (3PI - (PK - 2OFF))/2$$

OFF is an alignment constant settable via on board switches which must be set so $OFV \geq 0$ for good tracks. Also settable via on board switches is αMIN. If $\alpha < \alpha MIN$, KTL will be set and the track ignored if ALL is OFF.

$$\alpha_{MIN} \geq 0$$

$$\overline{ALL} \cdot PK < (PI + \alpha MIN) = KTL$$

$$\alpha_{MIN} < 0$$

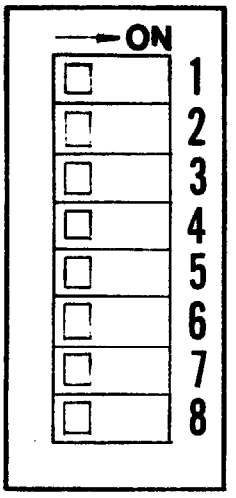
$$\overline{ALL} \cdot PK < (PI - \alpha MIN) = KTL$$

ECL-9 does not respond to any CAMAC commands.

Front Panel

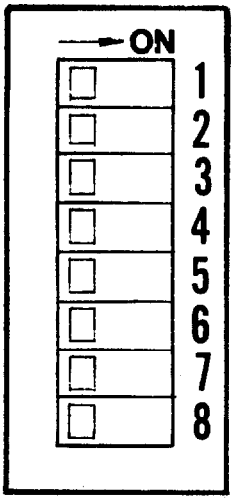
PI, PK	Input via 50-pin 3M connector, inputs are differential ECL levels. PI0 - PI10, pins 1 - 22; PK0 - PK10, pins 25 - 45 respectively.
OFV, Mα,Sα	Output via 34-pin 3M connector, outputs are differential ECL levels. 0FV0 - 0FV9, pins 1 - 20; Mα0 - Mα8, pins 21 - 38; Sα 1-bit pins 39 - 40. Sα=1 for pos and 0 for neg.
Mα MSB	Differential output via 2-pin lemo connector.
RDY1,RDY2	Output via 2-pin lemo connector, outputs are differential ECL levels. Logic 1 signifies a track and valied 0FV, Mα, and Sα.
ALL TRACKS	Front panel LED, on when all tracks are to be transmitted and α_{MIN} ignored. This is set via a front panel switch on ECL-8.

On Board Switches



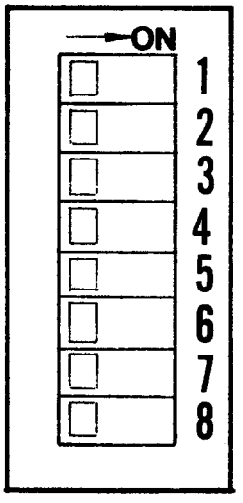
Offset 0

Offset 11 Bits
Switch On = Logical 1
Maximum Offset = 1334



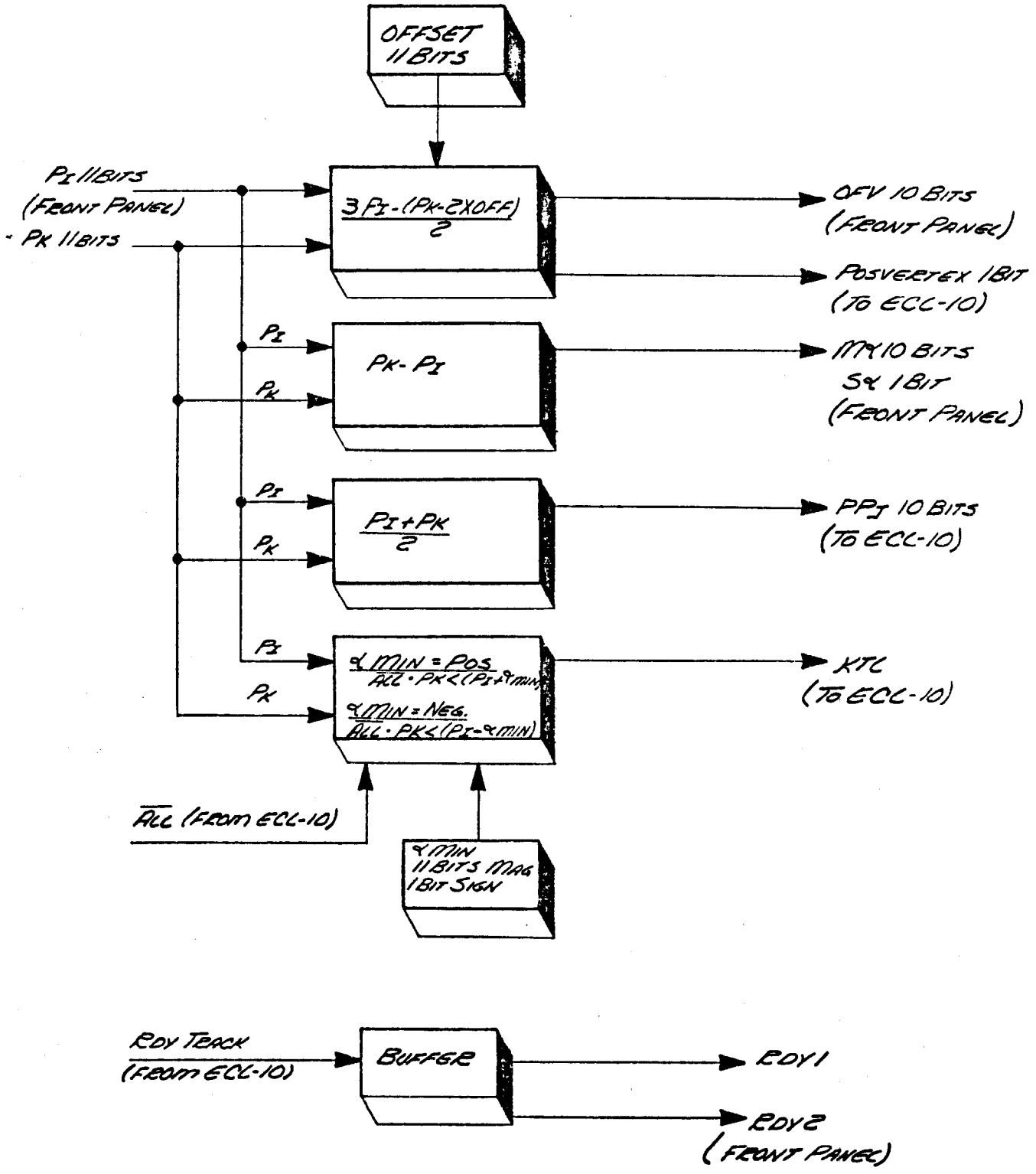
Offset 10
Not Used
Angle 0

Allowable Angle
11 Bits Magnitude
Switch On = Logical 1
Angle Sign — On = Pos, Off = Neg.



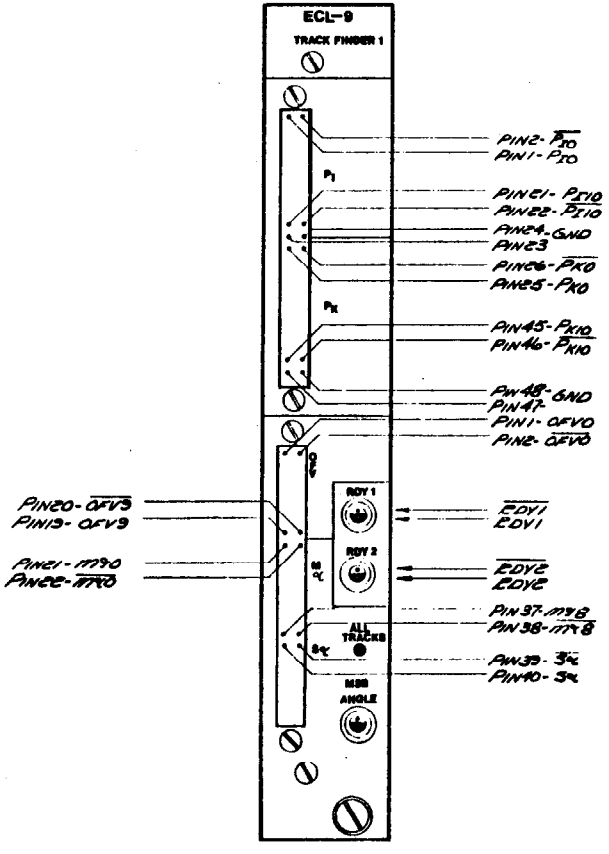
Angle 10
Angle Sign

ECL-9 TRACK FINDER-1



REVISIONS			
SYM	DESCRIPTION	DRAWN / APPD.	DATE / DATE

TM-0821
- 121 -



ITEM NO.	PART NO.	DESCRIPTION	QTY. REQ.

PARTS LIST

UNLESS OTHERWISE SPECIFIED			ORIGINATOR	KEN STEEPTOW	
FRACTIONS	DECIMALS	ANGLES	DRAWN	DAVE KLINE	11-16-78
±	±	±	CHECKED		
1. BREAK ALL SHARP EDGES 1/64 MAX.			APPROVED		
2. DO NOT SCALE DWG.			APPROVED		
3. DIMENSIONING IN ACCORD WITH USASI Y14.5 STD's.			USED ON		
√ MAX. ALL MACHINED SURFACES			MATERIAL-		

NATIONAL ACCELERATOR LABORATORY
U.S. ATOMIC ENERGY COMMISSION

BEAM SYSTEMS
ECL-9
FRONT PANEL LAYOUT

SCALE	FILMED	DRAWING NUMBER	REV.
FULL			

BRUNING 40-107—

FRONT

10-10115	18-10115	28-10115	38-10101	46-10101	56-10101
9-10115	17-10115	27-10115	37-10101	45-10101	55-10082
8-10182	16-10182	26-10182	36-10182	44-10182	54-10182
7-10182	15-10182	25-10182	35-10182	43-10182	53-10182
6-10181	24-10181	34-10181	52-10181		
5-10181	23-10181	33-10181	51-10181		
4-10182	14-10182	22-10182	32-10182	42-10182	50-10182
3-10166	13-SWITCH	21-SWITCH	31-SWITCH	41-10182	49-10182
2-10166	12-10166	20-10166	30-10166	40-10166	
1-10109	11-10104	19-10102	27-10109	39-10104	47-10195

FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	E516	TM-0821	- 123 -

SUBJECT

DOCUMENTATION OF: ECL-9

NAME: H. James Krebs

DATE: 11-29-78

REVISION DATE:

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-ED-104461
FRONT PANEL MACHING DRAWING	0880-MC-104384
FRONT PANEL ASSEMBLY	0880-MC-104462
FRONT PANEL ARTWORK	
MODULE FINAL ASSEMBLY	
P.C. CARD COMPONENT ASSEMBLY	
P.C. CARD DRILL DRAWING	
P.C. CARD PARTS LIST	0880-MA-104463
P.C. CARD MASTER ARTWORK	
BOARD OUTLINE	
SOFTWARE	

General Description - ECL-10 Track Finder-2

This double wide ECL/CAMAC module is a special purpose module used in conjunction with ECL-9 to find straight line segments in data from 3 evenly spaced wire chambers. This module receives middle chamber data (PJ) and uses it as a 10-bit address to a 4 x 768-bit RAM called the hit array. This location is loaded with IEV a 4-bit number (never 0000) that increments on each event and acts as an event identifier. After the projected middle chamber position (PPJ) is calculated by ECL-9 it is used to address the hit array. If the data at the PPJ location is equal to IEV for the present event a track is found. If the vertex is positive as calculated by ECL-9 a Ready Track signal is generated and used as a data output ready signal.

The chamber data must be loaded into the stacks and hit array in an ordered way (upstream first, downstream last). If PPJ > MAX PJ that has been received then KTH (K too high) is set to 1. If the Do Loop Controller ECL-8 has attempted to index either stack beyond data received the stack will raise its data exhausted (DE) level. This is received by this module at the PIDE or PKDE inputs and ITH (I too high) or KTH will be raised, as appropriate. In addition if the ALL TRACKS input is set off KTL (K too low) will be set if it is dictated by ECL-9 (see ECL-9 write up for more details). If none of the above conditions exist and a track has been found or not found, the CONT (continue) is set. The above signals are used by ECL-8 to determine the next indices.

The hit array has to be cleared through CAMAC when this module is first powered up. During normal operation after each event starting on master reset (MR), VETO+TRIG or DONE input 1/15 th of the hit array is cleared. Since there are 15 event identifiers all locations of the array with IEV from the last time a given IEV was used will have been cleared before the same IEV is used again.

CAMAC Commands

F0.A0 Read hit array RAM and increment CAMAC address pointer R/W1 - R/W4

F1 A0 Read status. R/W1 - R/W12

PI. PK RDY	TR ACK	DO NE	DV	ENA BLE	ALL	PK EX	PI EX	CO NT	KTH	KTL	ITH
R12											R1

F6 A0 Write RAM and increment CAMAC address pointer. R/W1 - R/W4

F24 A0 Disable control outputs (CONT, ITH, KTH, KTL), reset CAMAC address pointer, and set event counter (IEV) to 1.

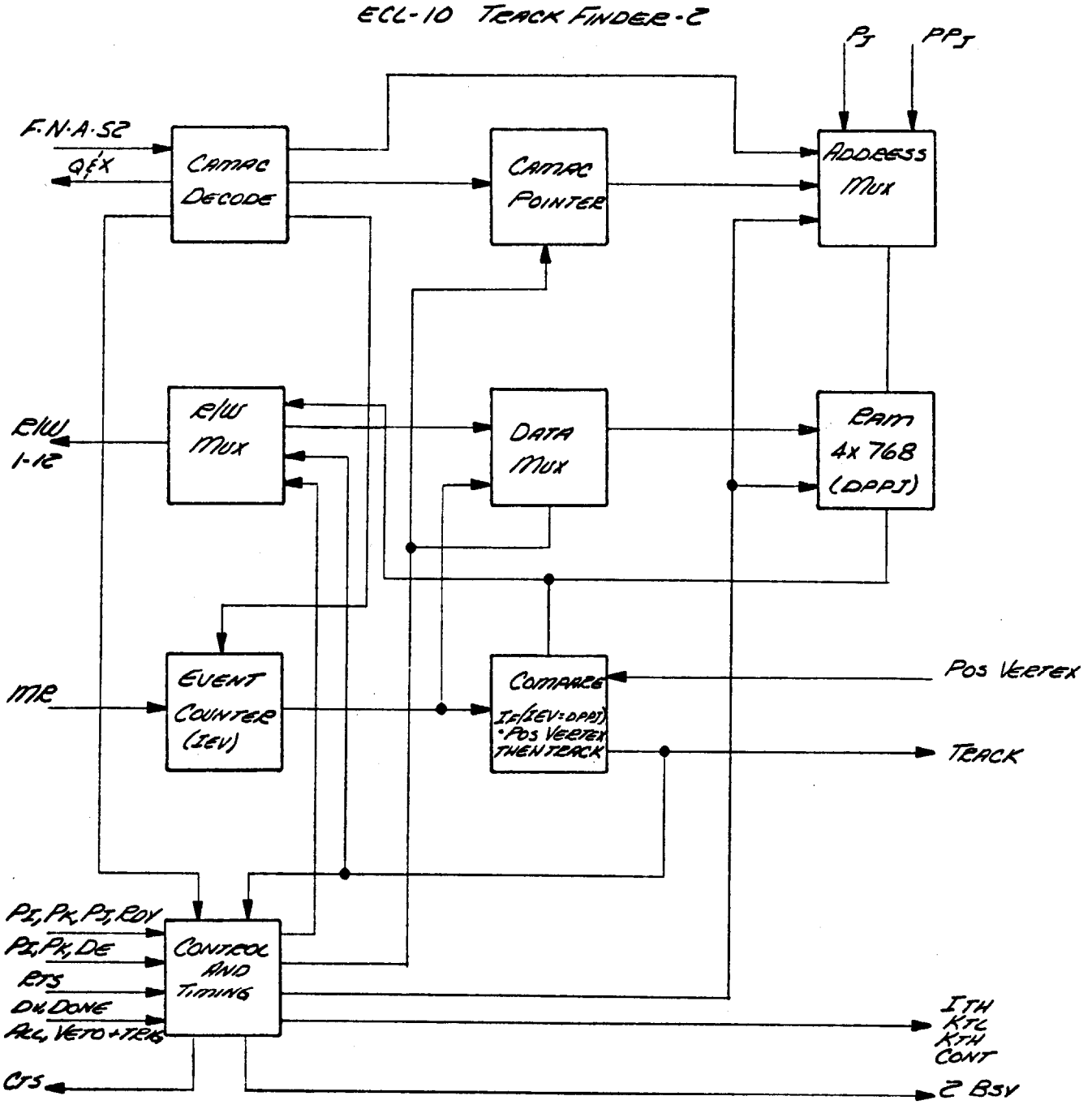
F25 A0 Overides disable to allow single step update of control outputs.

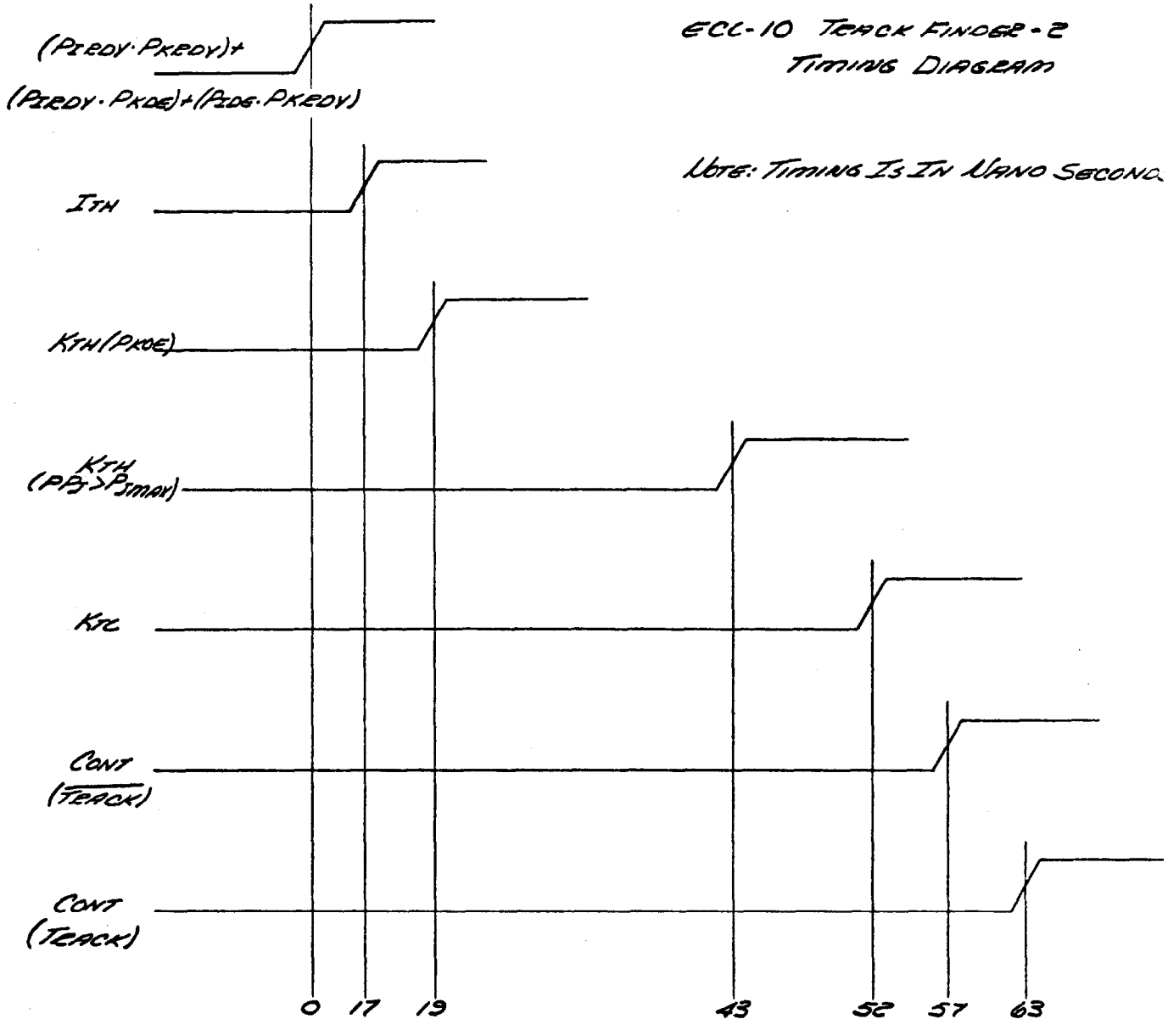
F26 A0 Enable control outputs

Front Panel

PI,PK, PJ RDY's	Inputs via 2-pin Lemo connectors, inputs are differential ECL levels. Signifies PI, PK, and PJ data is valid.
PI,PK	Inputs via 2-pin lemo connectors, inputs are differential ECL levels. Data exhausted signals from PI and PK stacks.
RTS	Request to send PJ data via 2-pin Lemo, differential ECL levels.
CTS	Clear to send PJ data output via 2-pin Lemo, differential ECL levels.
PJ	PJ input data via 20-pin 3M connector, inputs are differential ECL levels. PJ0-PJ9 pins 1 - 20.
DV	Data valid input from ECL-8, 2-pin Lemo, differential ECL.
DONE	Input from ECL-8, 2-pin Lemo, differential ECL levels.
VETO+TRIG	Abort signal input via 2-pin Lemo, differential ECL levels.
ITH,KTL, KTH,CONT, ALL	Control signal outputs and ALL input via 10-pin 3M connector to ECL-8, differential ECL levels.
ZBSY	Output via 2-pin Lemo, differential ECL levels, high during zeroing cycle of RAM.
ZBSY LED	On during zeroing cycle of RAM.
ENABLE LED	On when control outputs are enabled.

(Prepared by S. Bracker, R. Hance, T. Nash, K. Treptow - October 1, 1978)


ECL-10 TRACK FINDER-2
PJ
PPJ
F.N.A.S2
Q,X
CAMAC DECODE
CAMAC POINTER
ADDRESS MUX
R/W
I-12
R/W MUX
DATA MUX
RAM 4x768 (DPPJ)
MR
EVENT COUNTER (IEV)
COMPARE
IF(IEV=DPPJ) *POS VERTEX THEN TRACK
POS VERTEX
TRACK
PI, PK, PJ, RDY
PI, PK, DE
RTS
DH DONE
ARC, VETO + TRIG
CONTROL AND TIMING
ITH
KTC
KTH
CONT
CTS
2 BSY



ECC-10 IFRACK FINOGE-2
TIMING DIAGRAM

NOTE: TIMING IS IN NANO SECOND

ECL - 10 Track Finder -2 Charge Decode PROM

(10139)

CS (X). X) 256 BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: _____

P.O. NO.: _____

YOUR PART NO.: _____

DATE: _____

THIS PORTION TO BE COMPLETED BY SIGNETICS

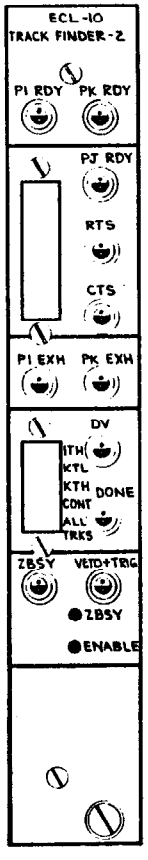
PART NO.: _____

S.D. NO.: _____

DATE RECEIVED: _____

WORD	INPUTS						OUTPUTS							
	A_4	A_3	A_2	A_1	A_0	ENABLE	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
F0 A0 0	0	0	0	0	0	0	1	1	0	0	0	0	0	1
F1 1	0	0	0	0	1	0	1	0	0	0	0	0	1	0
2	0	0	0	1	0	0								
3	0	0	0	1	1	0								
4	0	0	1	0	0	0								
5	0	0	1	0	1	0								
6	0	0	1	1	0	0								
7	0	0	1	1	1	0								
8	0	1	0	0	0	0								
9	0	1	0	0	1	0								
10	0	1	0	1	0	0								
11	0	1	0	1	1	0								
12	0	1	1	0	0	0								
13	0	1	1	0	1	0								
14	0	1	1	1	0	0								
15	0	1	1	1	1	0								
F16 16	1	0	0	0	0	0	1	1	0	0	0	1	0	0
17	1	0	0	0	1	0								
18	1	0	0	1	0	0								
19	1	0	0	1	1	0								
20	1	0	1	0	0	0								
21	1	0	1	0	1	0								
22	1	0	1	1	0	0								
23	1	0	1	1	1	0								
F24 24	1	1	0	0	0	0	1	1	0	0	1	0	0	0
F25 25	1	1	0	0	1	0	1	0	0	1	0	0	0	0
F26 26	1	1	0	1	0	0	1	0	1	0	0	0	0	0
27	1	1	0	1	1	0								
28	1	1	1	0	0	0								
29	1	1	1	0	1	0								
30	1	1	1	1	0	0								
31	1	1	1	1	1	0								
ALL	X	X	X	X	X	1	1	1	1	1	1	1	1	1

REVISIONS			
SYM	DESCRIPTION	DRAWN / APPD.	DATE / DATE



ITEM NO.	PART NO.	DESCRIPTION	QTY. REQ.

PARTS LIST

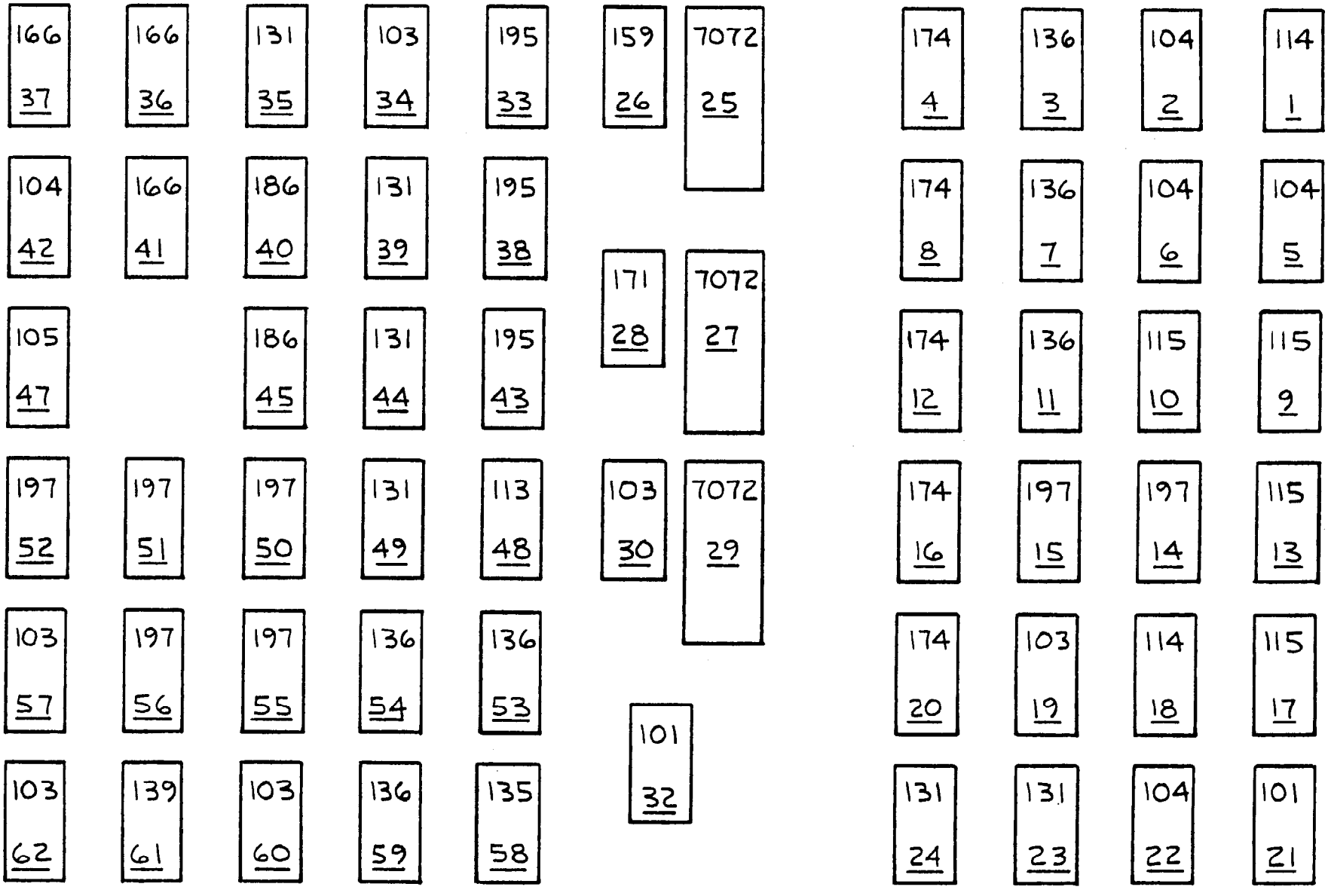
UNLESS OTHERWISE SPECIFIED			ORIGINATOR		
FRACTIONS	DECIMALS	ANGLES	DRAWN		
±	±	±	CHECKED		
1. BREAK ALL SHARP EDGES 1/64 MAX.			APPROVED		
2. DO NOT SCALE DWG.			APPROVED		
3. DIMENSIONING IN ACCORD WITH USASI Y14.5 STD's.			USED ON		
√ MAX. ALL MACHINED SURFACES			MATERIAL -		

NATIONAL ACCELERATOR LABORATORY
U.S. ATOMIC ENERGY COMMISSION

BEAM SYSTEMS
ECL-10
FRONT PANEL LAYOUT

SCALE	FILMED	DRAWING NUMBER	REV.

ECL-10 TRACK FINDER-2



FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	Exp. 516	TM-0821	- 132 -

SUBJECT

DOCUMENTATION OF:
ECL-10

NAME
H. James Krebs

DATE	REVISION DATE
6-23-78	

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-ED-104464
FRONT PANEL MACHING DRAWING	0880-MC-104343
FRONT PANEL ASSEMBLY	0880-MC-104465
FRONT PANEL ARTWORK	
MODULE FINAL ASSEMBLY	
P.C. CARD COMPONENT ASSEMBLY	
P.C. CARD DRILL DRAWING	
P.C. CARD PARTS LIST	0880-MA-104466
P.C. CARD MASTER ARTWORK	
BOARD OUTLINE	

ECL/CAMAC ECL-11
Single Index Do-loop Controller and
Test Transmitter
(General Purpose Test Module - Wire Wrapped - Double Width)

This is a special purpose test module to permit fast testing of memory stacks (ECL-4) and a Do-loop controller to transfer data from a stack (ECL-4) to the address input of an MLU (ECL-2). A block diagram illustrating the interconnections of these modules is shown in Fig. 1.

Modes of Operation: (Refer to Fig. 1)

Normal Test Mode:

In this mode data is transmitted from Stack #1 to Stack #2 at a relatively fast rate (≃ 20 MHz). After the data is transmitted it is then possible to make a comparison of the data contents of both stacks via the Camac dataway. The data comparison will determine, the highest burst rate of stack READS and WRITES, and other possible stack data transmit problems, when errors are encountered.

The start of the operation takes place by sending a reset pulse to the front panel reset (A, B or C) or the Camac dataway reset buss line. This reset pulse is buffered and output at the front panel 2-pin LEMOs labeled "EXT,PNT RST". These output pulses are used to reset the address pointers of both stacks. At the trailing edge of the reset pulse, ECL-11 outputs a Sequencial Ready (SEQ.RDY.) Pulse (internally adjustable pulse width)

and a Read Inhibit (RI) via front panel 2-pin LEMOs. This SEQ.RDY, when connected to Stack #1 as illustrated in Fig. 1, causes Stack #1 to output its first word along with an Output Ready (OR). When the "OR" is received at the ECL-11 input labeled "STK DATA RDY" the module outputs a "DATA RDY" to the "SWR" input of Stack #2 and the next "SEQ.RDY" to Stack #1. ECL-11 continues to issue "SEQ.RDY's" until a "DEX" is received from Stack #1, at which time the "RI" to Stack #2 is set to a logical zero and the process halts.

Sequence Test Mode:

This mode also allows a stack (ECL-4) to be Sequentially Read but at a Camac rate rather than a burst of "SEQ.RDY's". Connected as in Fig. 1, a "SEQ.RDY" will be output for each Camac F-25 issued to ECL-11, if a "DEX" from Stack #1 is present ECL-11 issues a no-Q response.

Another means to read out a stack in this mode is to send a 5-bit address to the random address input of a stack. This can be done by sending a Camac F-16 with the 5-bit address on R/W1 (LSB)-R/W5 (MSB). The F16 causes the 5-bit address output at the front panel 10-pin connector labeled "pointer" and is accompanied by a READY pulse (internally adjustable pulse width).

Loop Test Mode:

In this mode it is possible to do fast loop testing of stacks (ECl-4) to aid in scope troubleshooting.

This mode is identical to the normal test mode with the exception that upon receipt of a "DEX" from the stack, ECL-11

outputs on "EXT.PNT.RST" pulse to clear the stack READ address and starts another burst of "SEQ.RDY's".

Normal Mode:

This mode allows the user to transfer stack data to the address input of a preloaded memory lookup module MLU (ECL-2). And output a "match" or "no-match" condition depending upon the MLU output data and the stack "DEX". A "match" output is when the one bit MLU data ia received before a "DEX" is received from a stack otherwise a "no-match" pulse (internal adjustable pulse width) is output.

INPUTS:

All front panel inputs are two-pin LEMOs requiring differential ECL levels.

RESET A, B, C - initializes module, sends "EXT.PNT.RST" and "SEQ.RDY"or "PNT.RDY" at trailing edge of reset.

MASTER RESET - single ended ECL pulse from Pin 36R of ECL/CAMAC dataway. Functions identical to reset A, B and C.

STCK DATA RDY - Handshake signal for "SEQ.RDY" output pulse

STCK DATA EXH. - Input indicating the stack data is exhausted

MLU DATA - single bit data from a MLU

MLU DATA RDY - strobe input indicating the MLU data is ready

OUTPUTS:

All front panel outputs are differential ECL levels.

POINTER - 10-pin 3m connector, a 5-bit address used to random READ a stack

POINTER RDY - 2-pin LEMO, pointer strobe pulse (internal adjustable pulse width)

SEQ.RDY. - 2-pin LEMO sequential READ request to a stack (pulse width internally adjustable)

EXT.PNT.RST. - 2-pin LEMO, reset signal to initialize other modules, a buffered output of reset (A, B and C)

DATA OUT RDY - 1-pin LEMO, essentially a buffered STCK Data RDY signal

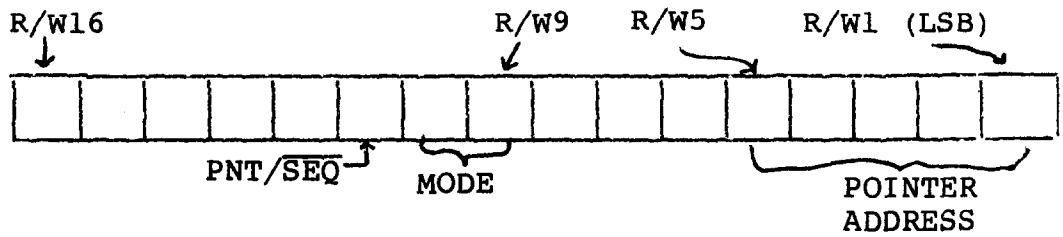
READ INH - 2-pin LEMO, Read Inhibit level to allow non-interrupted sequential writing to a stack

MATCH - 2-pin LEMO, indicating that the MLU data came before the stack "DEX"

NO-MATCH - 2-pin LEMO, internal adjustable pulse width indicating the stack "DEX" came before the MLU data

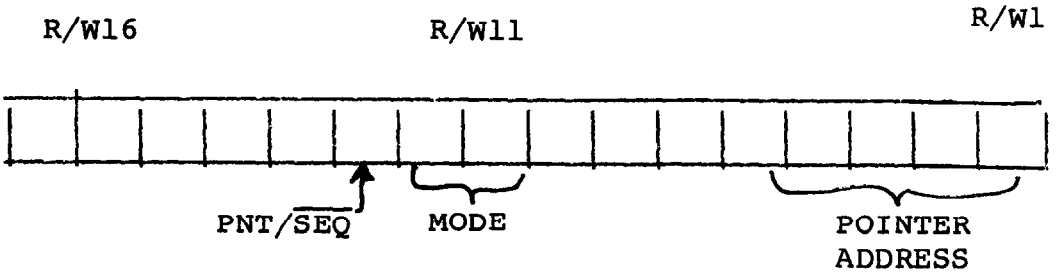
Camac Function Codes:

F0.A0 - Reads pointer address, test mode, and whether pointer RDY or SEQ.RDY has been selected



F9.A0 - Initializes module and outputs "EXT.PNT.RST."

F16.A0 - Write pointer address, test mode and outputs Pointer RDY or SEQ.RDY. Issues a Q-response if a DEX is not received



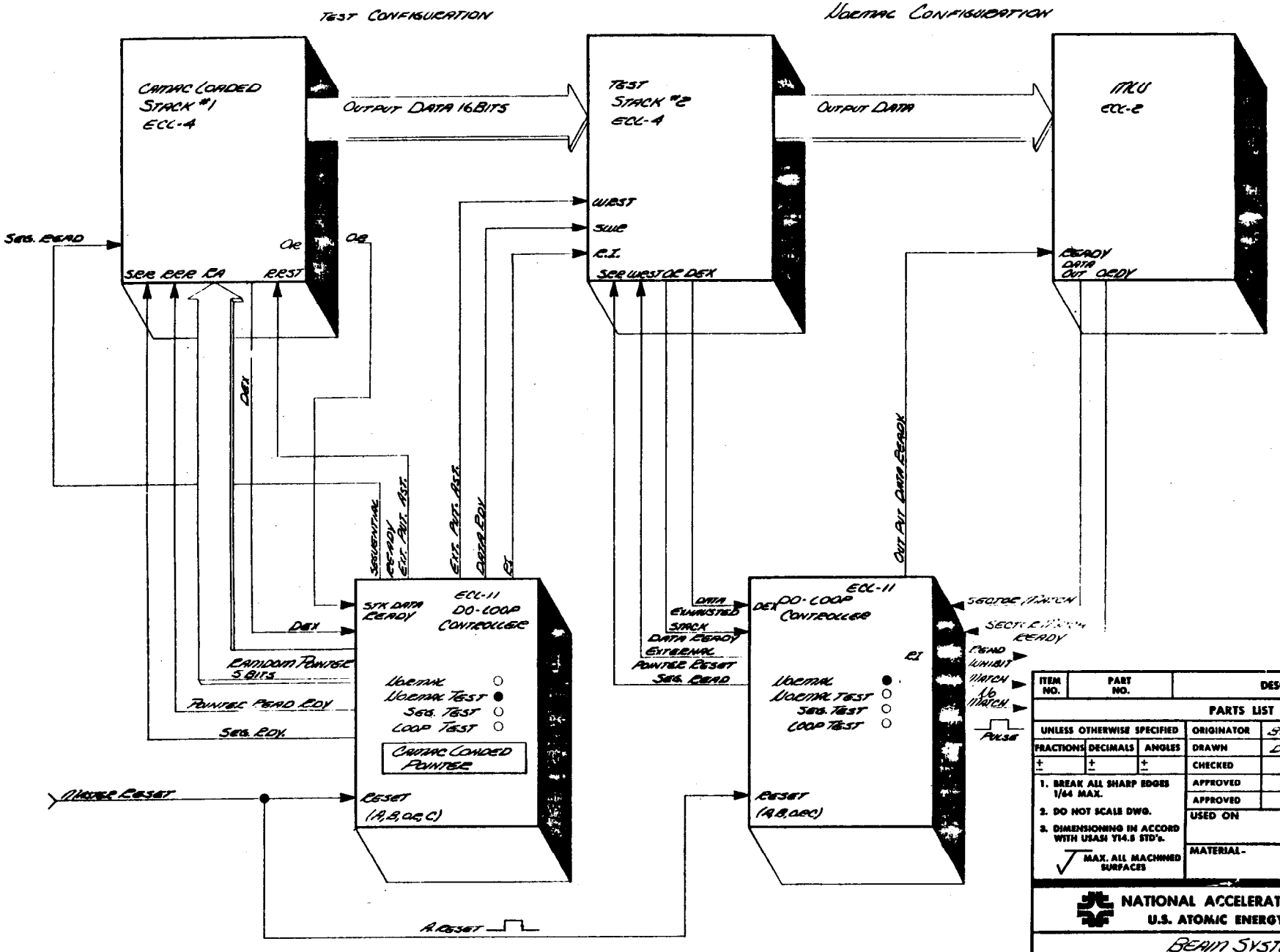
MODES OF OPERATION

	R/W	
	10	9
NORMAL	0	0
NORMAL TEST	0	1
SEQ. TEST	1	0
LOOP TEST	1	1

F25.A0 - Outputs a SEQ.RDY or a PNT.RDY depending on which was selected and issues a Q-response until "DEX" is received.

(Prepared by B. Haynes, 11/78)

REVISIONS			
SYM	DESCRIPTION	DRAWN / APPD.	DATE / DATE



ITEM NO.	PART NO.	DESCRIPTION	QTY. REQ.

PARTS LIST

UNLESS OTHERWISE SPECIFIED			ORIGINATOR	S. HAYNES	2/20/78
FRACTIONS	DECIMALS	ANGLES	DRAWN	D KLINE	11/15/78
±	±	±	CHECKED		
1. BREAK ALL SHARP EDGES 1/64 MAX.			APPROVED		
2. DO NOT SCALE DWG.			APPROVED		
3. DIMENSIONING IN ACCORD WITH USASI Y14.5 STD's.			USED ON		
√ MAX. ALL MACHINED SURFACES			MATERIAL -		

NATIONAL ACCELERATOR LABORATORY
U.S. ATOMIC ENERGY COMMISSION

BEAM SYSTEMS
ECL-11
BLOCK DIAGRAM

SCALE	FILMED	DRAWING NUMBER	REV.

BRUNING 40-107—

FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	Exp. 516	TM-0821	139

SUBJECT

DOCUMENTATION OF: ECL-11

NAME: H. James Krebs

DATE: 6-23-78

REVISION DATE:

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-EC-104342
FRONT PANEL MACHING DRAWING	0880-MC-104344
FRONT PANEL ASSEMBLY	0880-MC-104467
FRONT PANEL ARTWORK	
MODULE FINAL ASSEMBLY	
P.C. CARD COMPONENT ASSEMBLY	
P.C. CARD DRILL DRAWING	
P.C. CARD PARTS LIST	0880-MA-104468
P.C. CARD MASTER ARTWORK	
BOARD OUTLINE	

ECL-CAMAC ECL-12

Quad Four-Bit Function Module (Scaler)

(General Purpose Module - Multiwire- Double Width)

Introduction

This module was designed primarily for scaling of internal operations and loops as well as the frequency of occurence of various internal conditions in a trigger processor. Examples of the latter in the recoil trigger are failed tracks, non-proton tracks, and the number of different vertices. The results may, on each event, also be transmitted via CAMAC to the on-line computer to monitor changes in such things as success ratios that would indicate a hardware problem. In this application the modules are normally reset to zero at the beginning of each event.

Applications

In the primary application of this module as a scaler, each of the four sections performs scaling (or adding) of up to 4 bits of input data. The output of each section is 4 bits. An overflow bit, one per section, is set via a jumper selectable option when an output equals or exceeds a count of 1, 2, 4, 8, or 16. The user may select, via another switch option, to freeze the output and overflow of a given section at the occurence of an overflow condition or to use the overflow bit to cascade the sections providing up to a 16-bit counter within one module. The scaler can count as fast as 40 MHz.

Each section uses an ECL-10181, 4-bit arithmetic logic unit (ALU) to scale input data. By using this ALU and on board switches this module is additionally capable of performing several arithmetic and logic functions such as incrementing, decrementing and complementing a single input word. It can also be used for adding, subtracting, normal and exclusive ORing/NORing, ANDing and NANDing of two four-bit input words.

The two input registers in each section may be read and written via CAMAC. The output of each ALU is also CAMAC readable. Each section has individual input Readys and Clears. There is a General Module Clear and a General Input Ready. This general Ready may be ORed to any input Ready via on board switches.

General Description

This module consists essentially of 4 arithmetic logic units, each capable of handling 4-bit words. The 4-bit output and the "OFLO" output are a function of two 4-bit front panel inputs, or alternatively one 4-bit front panel input and the current 4-bit output. (The latter allows scaling).

The 4 input bits are connected to the front panel via a 20 contact (top 8 are input) "I/O" connector. The least significant bit may also be entered through an individual LEMO twinax connector labeled LSB.

The output function produced is determined by a dip switch (one per ALU) and on board jumper options. One option, for example, is to connect OFLO to any one of the four output bits or carry and have the occurence of that OFLO lock out additional

inputs. Another option is to set all outputs to 1 on OFLO.

The simplified logic diagram of Fig. 2 shows two input registers per ALU. The eight input registers (only 4 shown) are CAMAC writeable and readable; the outputs are CAMAC readable. Each section is individually resetable, i.e., Reg's A and B set to zero; via front panel reset or CAMAC F9. Input data may strobed in by individual input Ready's "IR's" only, or, if selected, a logical OR of "IR" and "GR".

A description of the front panel connectors, controls and LEDs is given in Fig. 1.

The functions generated are listed in Table I and on the schematic diagram.

Circuit Description

Since there are four sections to this module an explanation of one shall suffice. The section utilizing ALU A7 (see schematic diagram) operates as follows.

Clear (CLR), received at A14-12 and 13 (the characters before the dash represent the IC designation, whereas the numbers following the dash are pin numbers) causes a high level to be sent to B13-10 resulting in a high at A9-1 and A8-1 and forces A9-9 and A8-9 low thru B9 and B8 respectively. This condition sets A9 and A8 outputs low. A high on B13-11 caused by front panel push button Clear (CLR), crate reset (dataway pin 36R going high), or power on; has the same effect as that caused by B13-10 going high.

Input Ready (IR), received at A13-4 and 5 causes a high

at A13-3 which is wire OR'ED with B13-3 and inverted at A12-2. A12-2 is connected to B8-14 and which is enabled, via C12-11, by A6-1 (S1). When S1 is open, the parallel LED (I2 on front panel) turns on indicating the output is a function of two front panel inputs I1 and I2. C12-10 is now low enabling B8-13 and 14 and disabling B9-14. A low on both B8-13 and 14, i.e. a coincidence of section 3 and 4 Readys, causes B8-15 to go high, thus B8-2 and B9-2 go low. If there is no Clear in progress and if D6-2 is low, B8-3 and B9-3 go high transferring data at the input of A8 and A9 to their respective outputs. The input to A9 came from section 1 inputs whereas the input to A8 came from section 2 input (A6-1 and 1b) because A10-7 was enabled and B10-9 disabled. When S1 (A6-1 and 1b) is closed, C12-11 is high enabling B10 and disabling A1D. In this configuration, the next output is a function of the current output and the next input.

Overflow (OFLO) is a jumper selectable output which may be any of the 4 output bits or carry OFLO is enabled by S2. An overflow on D6-6 causes a high level on D9-5 and D10-5 inhibiting further clock signals to C8-9 and C9-9 thus putting it in a hold mode.

The output ready (OR) A5-6 and A5-7 may be CAMAC inhibited or inabled by B6-15. The other half of B6 coupled with one third of C12 constitute an adjustable one shot which determined the duration of OR absence. Timing is controled by the RC combination on B6-2. Assuming the logic swing on B6-2 is -0.875 v and -1.75 v the pulse width is approximately $t = 1.6\ R_T C$.

The CAMAC function codes and responses are shown below:

Specifications

Power Requirements

-5.2 AT ———————— AMPS

-2.0 AT ———————— AMPS

Input

Signal levels - ECL differential

Input impedance - 110 differential

CMRR - ±1 volt

Output

Single levels ECL differential

Output impedance - Open emitters with 560 pull down resistors to -5.2 V

(Prepared by M. Haldeman, 11/78)

4.1 CAMAC FUNCTIONS

CAMAC COMMAND	FUNCTION	RESPONSE Q	RESPONSE X
N·F0·A(Y)	READ REGISTER A, SECTION (Y)	1	1
N·F1·A(Y)	READ REGISTER B, SECTION (Y)	1	1
N·F2·A(Y)	READ OUTPUT	1	1
N·F9·A(Y)·S1	SET REGISTERS A & B TO ZERO, SECTION (Y)	1	1
N·F16·A(Y)S1	WRITE REGISTER A, SECTION (Y)	1	1
N·F17·A(Y)S1	WRITE REGISTER B, SECTION (Y)	*	1
N·F24·A(Y)·S1	DISABLE [OR], SECTION (Y)	1	1
N·F25·A(Y)S1	ENABLE [OR], SECTION (Y)	1	1

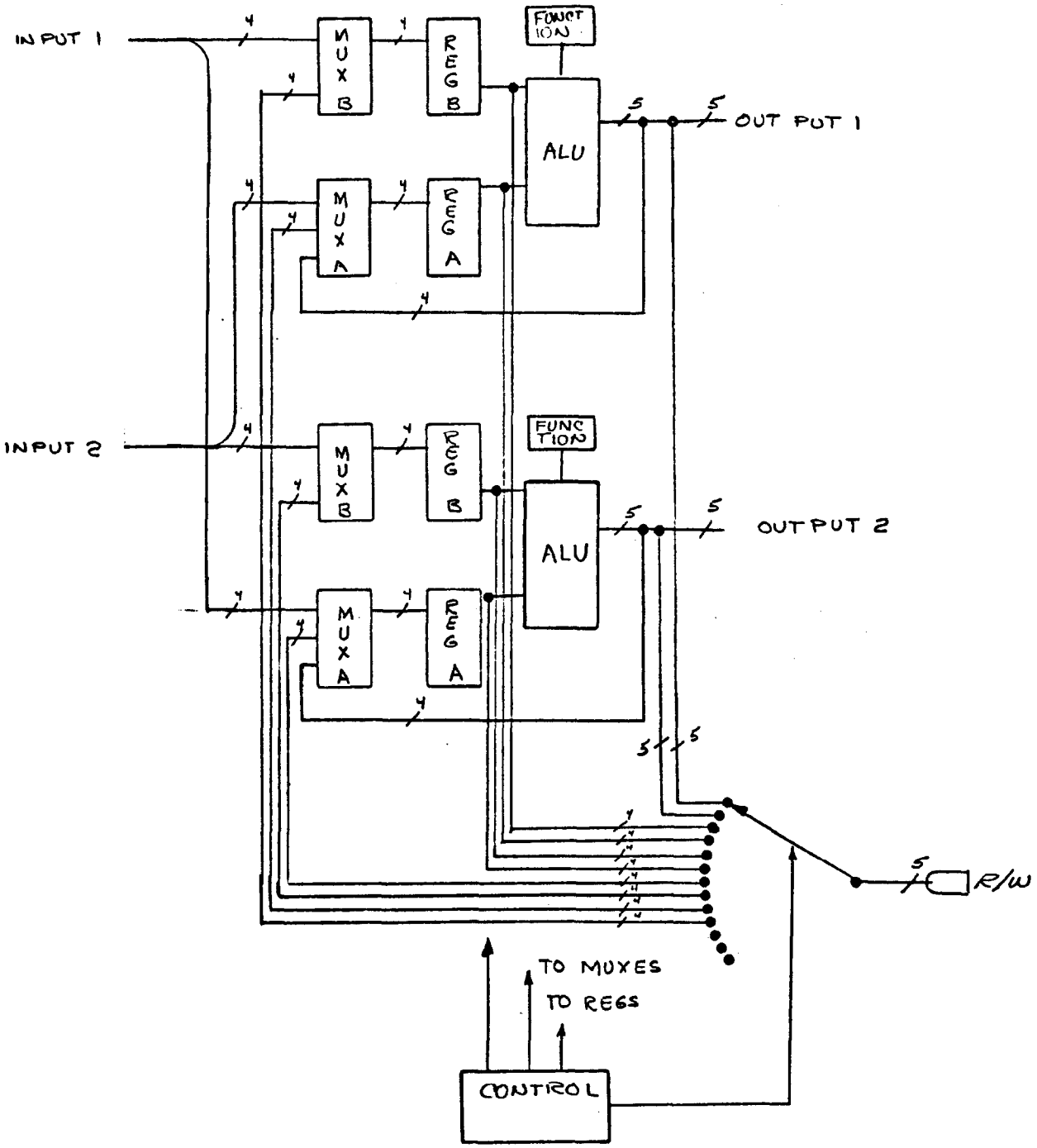
(Y) = 1,2,3 OR 4 = SECTION NUMBER OF QUAD MODULE
* = 0 IF A6-1 IS CLOSED; 1 IF A6-1 is OPEN

4.0 FUNCTION SWITCH TABLE

S_N = SWITCH POSITION "N"
1 = ON (SHORTED)
0 = OFF (OPEN)
X = DON'T CARE

				OUTPUT		
				$S_4 = 1$ LOGIC MODE	$S_4 = 0$ ARITHMETIC MODE	
S_5	S_6	S_7	S_8	$S_3 = X$	$S_3 = 0$	$S_3 = 1$
0	0	0	0	$\bar{B}$	B	B PLUS 1
0	0	0	1	$\bar{A}+\bar{B}$	B PLUS $\bar{A}\cdot B$	B PLUS $\bar{A}\cdot B$ PLUS 1
0	0	1	0	$A+\bar{B}$	B PLUS $A\cdot B$	B PLUS $A\cdot B$ PLUS 1
0	0	1	1	HIGH	2B	B PLUS B PLUS 1
0	1	0	0	$\bar{A}\cdot\bar{B}$	A+B	(A+B) PLUS 1
0	1	0	1	$\bar{A}$	(A+B) PLUS $\bar{A}\cdot B$	(A+B) PLUS $\bar{A}\cdot B$ PLUS 1
0	1	1	0	$\overline{A\oplus B}$	A PLUS B	A PLUS B PLUS 1
0	1	1	1	$\bar{A}+B$	(A+B) PLUS B	(A+B) PLUS B PLUS 1
1	0	0	0	$A\cdot\bar{B}$	$\bar{A}+B$	$\bar{A}+B$ PLUS 1
1	0	0	1	$A\oplus B$	B MINUS A MINUS 1	B MINUS A
1	0	1	0	A	$(\bar{A}+B)$ PLUS $A\cdot B$	$(\bar{A}+B)$ PLUS A PLUS 1
1	0	1	1	A+B	$\bar{A}+B$ PLUS B	$(\bar{A}+B)$ PLUS B PLUS 1
1	1	0	0	LOW	MINUS 1 (2's COMPLEMENT)	ZERO
1	1	0	1	$\bar{A}\cdot B$	$\bar{A}\cdot B$ MINUS 1	$\bar{A}\cdot B$
1	1	1	0	$A\cdot B$	$A\cdot B$ MINUS 1	$A\cdot B$
1	1	1	1	B	B MINUS 1	B

S_1	S_2	
0	X	A REGISTER = 2nd FRONT PANEL INPUT
1	0	A REGISTER = PREVIOUS FUNCTION OUTPUT; HOLD OUTPUT AT 1111 ON OVERFLOW
1	1	A REGISTER = PREVIOUS FUNCTION OUTPUT; NO HOLD ON OVERFLOW



SIMPLIFIED LOGIC FOR INPUTS 1 & 2

FIG 2

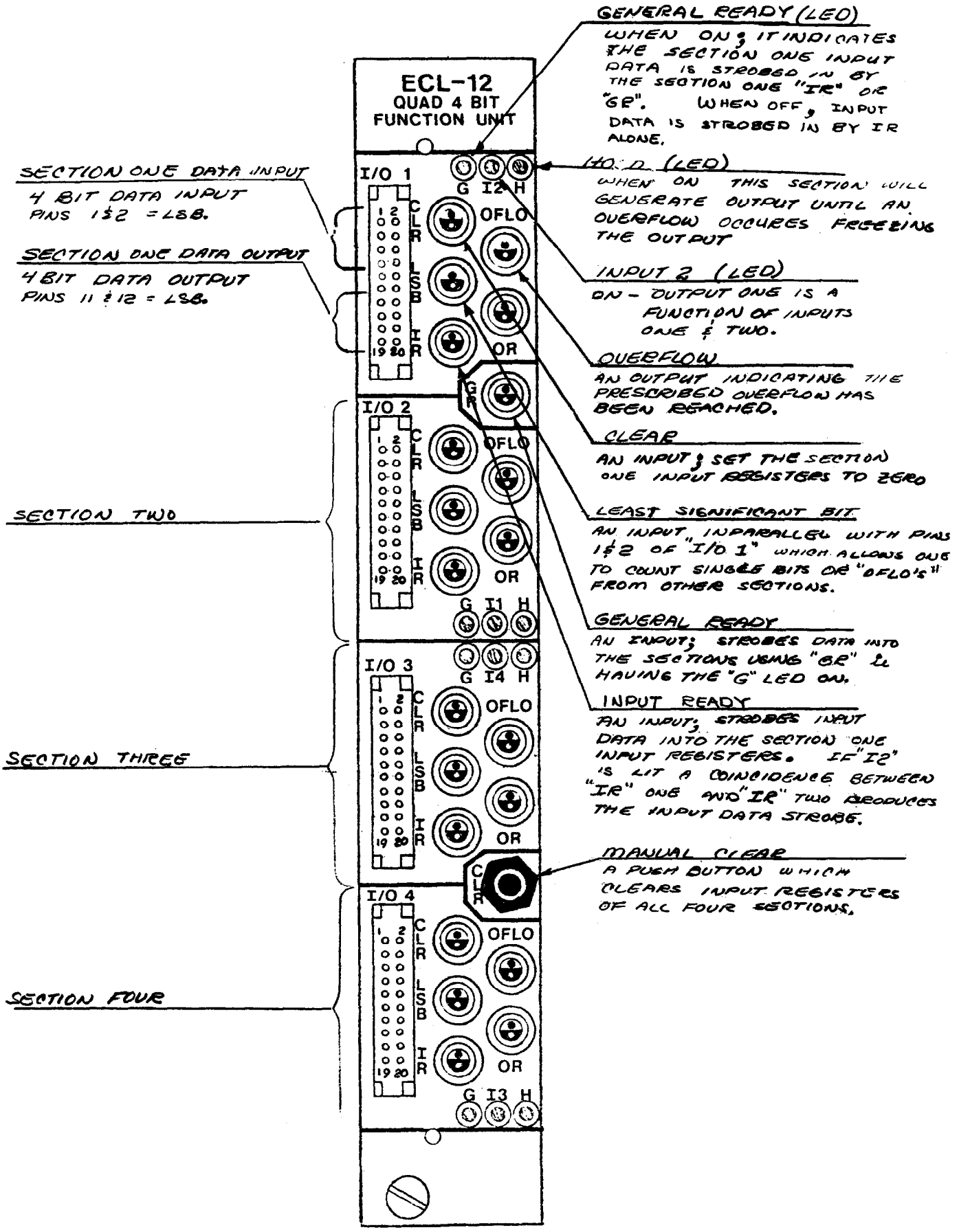

ECL-12
QUAD 4 BIT
FUNCTION UNIT
I/O 1
I/O 2
I/O 3
I/O 4
G I2 H
G I1 H
G I4 H
G I3 H
OFLO
OR
CLR
LSB
IR
GR
SECTION ONE DATA INPUT
4 BIT DATA INPUT
PINS 1 & 2 = LSB.
SECTION ONE DATA OUTPUT
4 BIT DATA OUTPUT
PINS 11 & 12 = LSB.
SECTION TWO
SECTION THREE
SECTION FOUR
GENERAL READY (LED)
WHEN ON; IT INDICATES THE SECTION ONE INPUT DATA IS STROBED IN BY THE SECTION ONE "IR" OR "GR". WHEN OFF, INPUT DATA IS STROBED IN BY IR ALONE.
HOLD (LED)
WHEN ON THIS SECTION WILL GENERATE OUTPUT UNTIL AN OVERFLOW OCCURES FREEZING THE OUTPUT
INPUT 2 (LED)
ON - OUTPUT ONE IS A FUNCTION OF INPUTS ONE & TWO.
OVERFLOW
AN OUTPUT INDICATING THE PRESCRIBED OVERFLOW HAS BEEN REACHED.
CLEAR
AN INPUT; SET THE SECTION ONE INPUT REGISTERS TO ZERO
LEAST SIGNIFICANT BIT
AN INPUT, INPARALLEL WITH PINS 1 & 2 OF "I/O 1" WHICH ALLOWS ONE TO COUNT SINGLE BITS OR "OFLO's" FROM OTHER SECTIONS.
GENERAL READY
AN INPUT; STROBES DATA INTO THE SECTIONS USING "GR" & HAVING THE "G" LED ON.
INPUT READY
AN INPUT; STROBES INPUT DATA INTO THE SECTION ONE INPUT REGISTERS. IF "I2" IS LIT A COINCIDENCE BETWEEN "IR" ONE AND "IR" TWO REPRODUCES THE INPUT DATA STROBE.
MANUAL CLEAR
A PUSH BUTTON WHICH CLEARS INPUT REGISTERS OF ALL FOUR SECTIONS.

FIG 1

FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	E516	TM-0821	149

SUBJECT

DOCUMENTATION OF: ECL-12

NAME: H. James Krebs

DATE	REVISION DATE
11-22-78	11-22-78

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-EE-104469
FRONT PANEL MACHING DRAWING	0880-MC-104470
FRONT PANEL ASSEMBLY	0880-MC-104471
FRONT PANEL ARTWORK	0880-MC-104472
MODULE FINAL ASSEMBLY	0880-MD-104473
P.C. CARD COMPONENT ASSEMBLY	0880-MD-104474
P.C. CARD SILK SCREEN ARTWORK	0880-MD-104475
MODULE PARTS LIST	0880-MA-104476
P.C. CARD MASTER ARTWORK (POWER & GROUND)	0880-MD-104477
BOARD OUTLINE	0880-MC-104478
PHOTO REDUCTIONS	FP-32
MULTIWIRE IBM CARD DECK	
SOFTWARE	

ECL/CAMAC ECL-13

Vertex Parameter Module

(Special Purpose Module to be used in E516 Recoil Processor

Wire Wrapped - Double Width)

General Description:

This module has for its input, the most recent hadronic vertex. It stores this 10-bit word into a register called V_i. Upon the arrival of a new hadronic vertex, the contents of V_i is shifted into another register called $V_{(i-1)}$. Upon the arrival of another new hadronic vertex, the contents of $V_{(i-1)}$ is shifted into a register called $V_{(i-2)}$. There is a fourth register called V'. This register will store the most recent hadronic vertex (V_i) as the most upstream vertex to date (V') upon receipt of a store and store ready signal from the vertex MLU.

With these vertices in memory, the module calculates and outputs on a 34-pin connector called ODA the following quantities:

$\delta_{(i-1)}$, the 3 LSB of $|V_i - V_{(i-1)}|$.
δ'_H bits 7, 8 and 9 of $|V_i - V'|$
δ'_L bits 1, 2, 3 and 4 of $|V_i - V'|$
S', the sign of $V_i - V'$. 1 if > 0, 0 if ≤ 0

The quantity $\delta_{(i-2)}$ is also calculated, but not connected to the front panel. $\delta_{(i-2)} = |V_i - V_{(i-2)}|$

The last major function of this module is to store the parameters cos θ, E, p and S upon receipt of a store and store ready signal from the vertex MLU.

cos θ is a 7-bit word stored in a register called cos θ'

E is a 6-bit word stored in a register called E'

P is a 1-bit word stored in a register called P'

S is a 1-bit word stored in a register called S'

Cos θ' and E' are output on a 34-pin connector called ODB and are fed to the M_x MLU. P' and S' are output on 2-pin LEMOs.

FIGURE 1

INPUTS AND OUTPUTS

Inputs

EPR1 Rdy	Electron Proton Ready 1	2-pin Lemo
EPR2 Rdy	Electron Proton Ready 2	2-pin Lemo
EPR3 Rdy	Electron Proton Ready 3	2-pin Lemo
V, S_α Rdy		2-pin Lemo
NH	Non-Hadron	2-pin Lemo
Store		2-pin Lemo
STORE Rdy		2-pin Lemo
S		2-pin Lemo
P	Proton	2-pin Lemo
V,E,cos	50-pin connector (25 signals possible)	

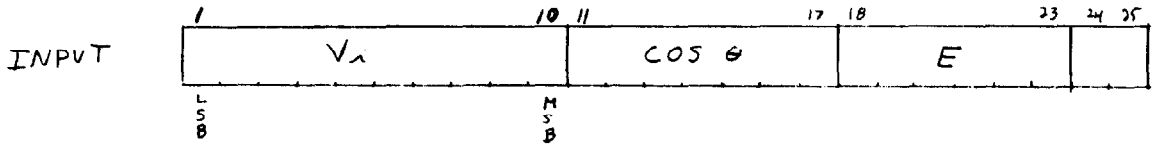
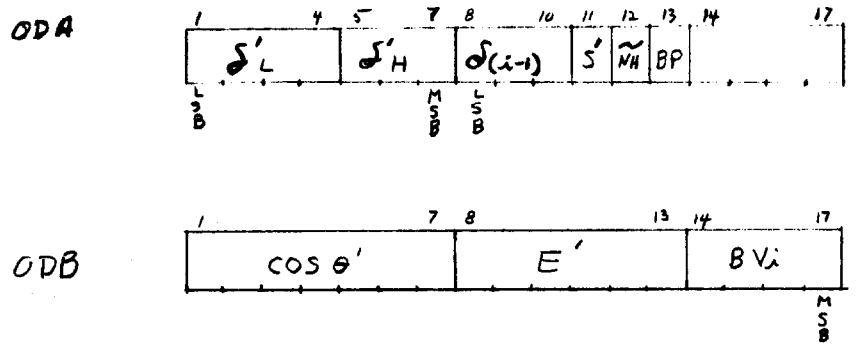


FIGURE 1 (cont'd)

Outputs

OR1	Output Ready 1	2-pin Lemo
OR2	Output Ready 2	2-pin Lemo
BNH	Buffered NH	2-pin Lemo
BNH	Buffered NH	2-pin Lemo
B(V, S_α)Rdy	Buffered (V, S_α)Rdy	2-pin Lemo
B S_α	Buffered S_α	2-pin Lemo
S'	Sign of (V_i-V')	2-pin Lemo
ODA	34-pin Conn.	
ODB	34-pin Conn.	



Modes of Operation: (See Fig. 1 for data format)

1) Reset - Sets all latches to zero and sets both output readies low.

2) Non-Hadronic Event - NH+($\overline{EPR1}$ + $\overline{EPR2}$ + $\overline{EPR3}$ + $\overline{V,S\alpha}$ Ready). Outputs buffered NH only.

3) For every (V,Sα) Ready, NH will be stored as NH'.

4) First Hadronic Event -
   - Requires four simultaneous input readies and not NH: (EPRI•EPR2•EPR3•(V,Sα)Rdy•$\overline{NH}$)
   - Stores V_i (most recent vertex)
   - Enters V_i as V' (most upstream vertex)
   - Stores parameters (cos θ, E, P and Sα)
   - δ_L' is gated off (will be zero)
   - The 4 MSB of V_i are buffered out
   - OR1 will go high after V_i is clocked in and enough time has elapsed for calculations to be completed. OR1 will then go low as soon as one of the input readies (EPR1, EPR2, EPR3, (V, Sα)) goes away.
   - OR2 will go high after parameters are stored and will remain high until the next store command is received.

5) Hadronic Event (other than first)

- The 4 MSB of V_i are buffered out.
- Requires four simultaneous readies and not NH:
  (EPR1•EPR2•EPR3•(V, Sα) Rdy•$\overline{NH}$)
- Stores V_i and calls it V_i
- Shifts old V_i and calls it $V_{(i-1)}$
- Shifts old $V_{(i-1)}$ and calls it $V_{(i-2)}$
- Calculates and outputs the three least significant bits of $|V_i - V_{(i-1)}|$. An overflow condition is shown by all bits high.
- Calculates, but does not output the three least significant bits of $|V_i - V_{(i-2)}|$. This also has an overflow condition shown by all bits high.

  Calculates $V_i - V'$ and outputs this in two parts:

  part 1) The four least significant bits are called δ' low

  part 2) Bits 7, 8, and 9 are called δ' high

  Both of these signals have an overflow condition shown by all bits high.
- Outputs S', the sign of $(V_i - V')$ 1 if > 0, 0 if $\leq$ 0
- OR1 will go high when all of the above conditions are true and will stay high until one of the input readies (EPR1, EPR2, EPR3, (V, Sα)) goes away.

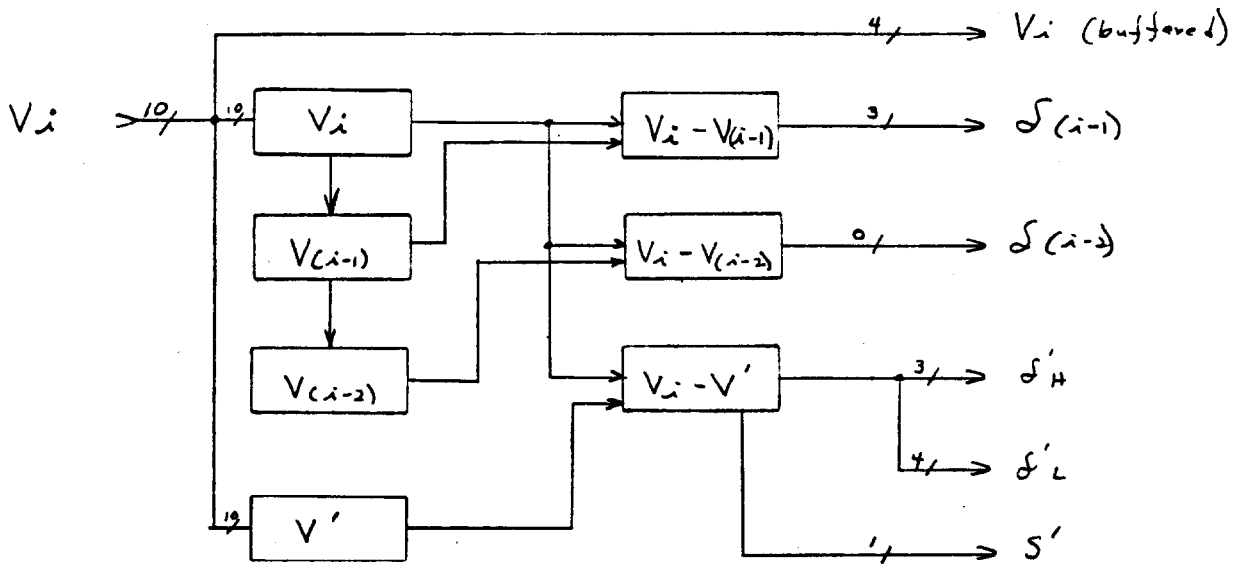
The module now waits for a store command from the vertex MLU. The following sequence requires STORE and STORE READY signals from the vertex MLU.

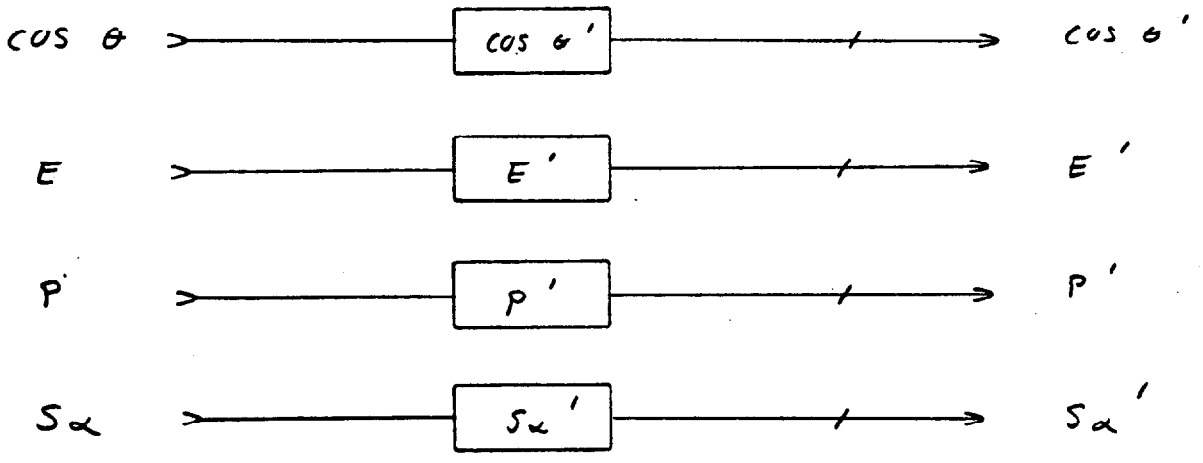
- Stores V_i and calls it V' (most upstream vertex)
- Stores the parameters cos θ, E, S_α and P and outputs them as cos θ', E', S_α', P'
- OR2 will go low when the store command is received, and will go back high when the store procedure is complete.
- Buffered and ungated outputs are supplied for P, S_α, (V,S_α) Rdy, NH.

(Prepared by T. Soszynski, 11/78)

ECL - 13

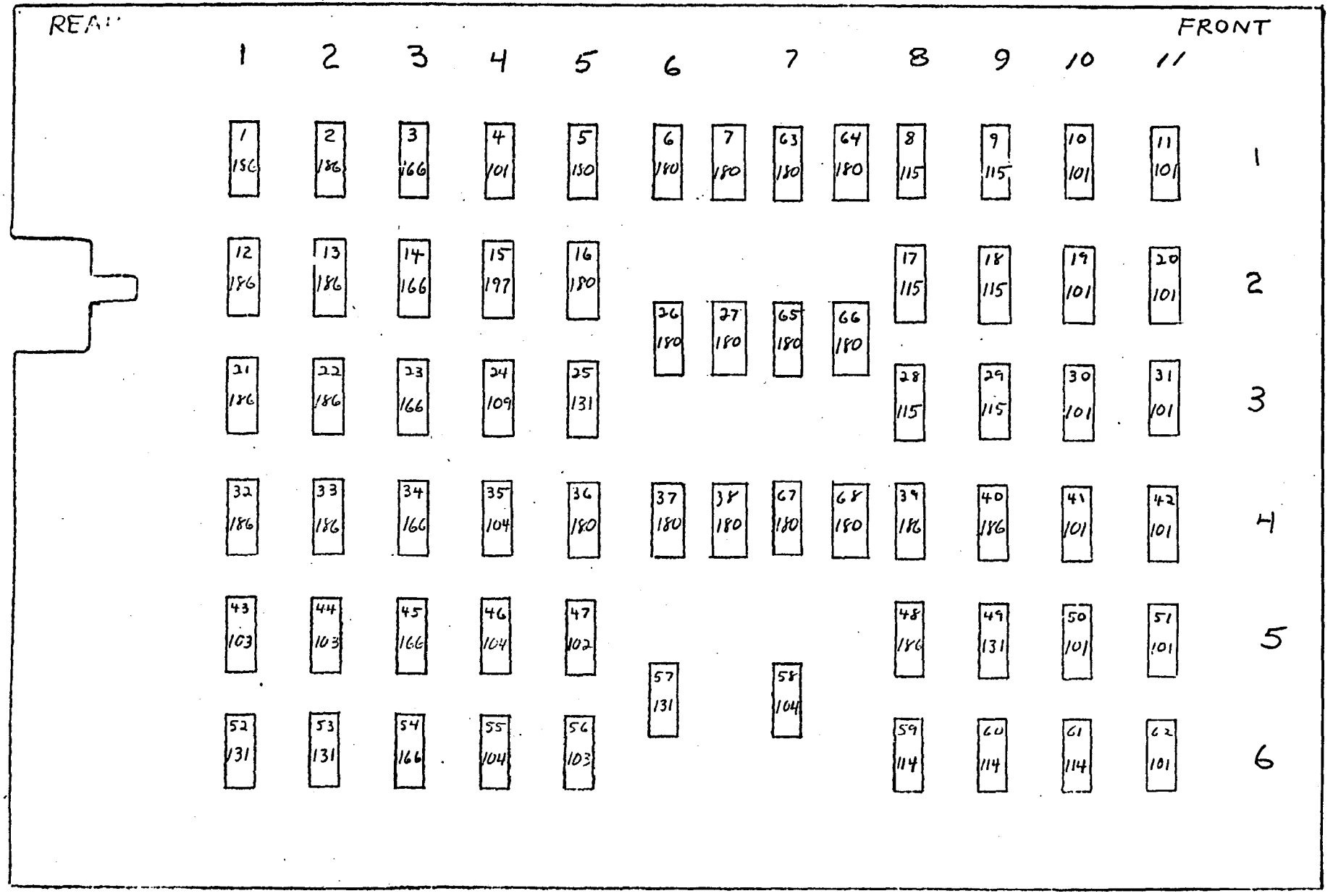
SIMPLIFIED BLOCK DIAGRAM



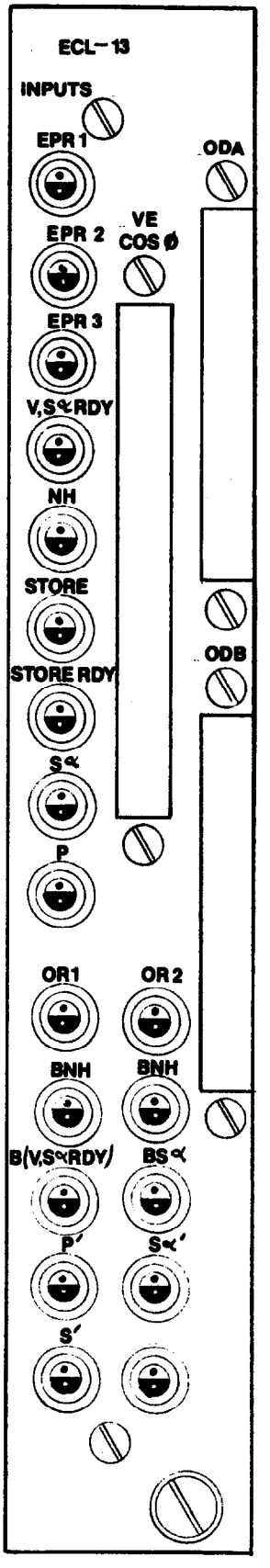


ECL-13 I.C. LAYOUT

TOP



ECL-13 FRONT PANEL LAYOUT



DMK 11/78

FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	Exp. 516	TM-0821	160

SUBJECT

DOCUMENTATION OF: ECL-13

NAME: H. James Krebs

DATE: 6-23-78

REVISION DATE:

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-ED-104484
FRONT PANEL MACHING DRAWING	0880-MC-104485
FRONT PANEL ASSEMBLY	0880-MC-104486
FRONT PANEL ARTWORK	
MODULE FINAL ASSEMBLY	
P.C. CARD COMPONENT ASSEMBLY	
P.C. CARD DRILL DRAWING	
P.C. CARD PARTS LIST	0880-MA-104487
P.C. CARD MASTER ARTWORK	
BOARD OUTLINE	

ECL/CAMAC Module ECL-14

General Logic Module (General Purpose Module -

PC Board - Single Width)

General Description

This single width ECL CAMAC module was designed to allow the option of selecting one of four logic functions in each of three sections listed below:

1st $[(A_i \cdot B_i) \cdot C_i] G_i \cdot K_i = Q_i$

2nd $[(A_i + B_i) \cdot C_i] G_i \cdot K_i = Q_i$

3rd $[(A_i \cdot B_i) + C_i] G_i \cdot K_i = Q_i$

4th $[(A_i + B_i) + C_i] G_i \cdot K_i = Q_i$

Where K = CAMAC enable

i = Subscript indicating Section 0, 1, or 2 of the module

The module has two identical logic sections with differential inputs (A_i, B_i, C_i), Gate (G_i), and a differential output Q_i. The third logic section is identical but does not include the Gate (G_i) input.

The logic functions for each section is independently selectable using a switch on the PC board. LED indicators on the front panel display the selected logic function for each section as well as status of the input enable latch and the output set latch.

The status of the module can be read via CAMAC. CAMAC commands can also be used to over-ride the inputs and set the output to an ECL logical one or zero.

CAMAC Instructions

F0.A0 Reads logic gate inputs A_i, B_i, C_i, G_i

R/W16 R/W1

		K_2	C_2	B_2	A_2	G_1	C_1			B_1	A_1	G_0	C_0	B_0	A_0

F1.A0 Reads logic switch settings

R/W16 R/W1

		4_2	3_2	2_2	1_2	4_1	3_1			2_1	1_1	4_0	3_0	2_0	1_0

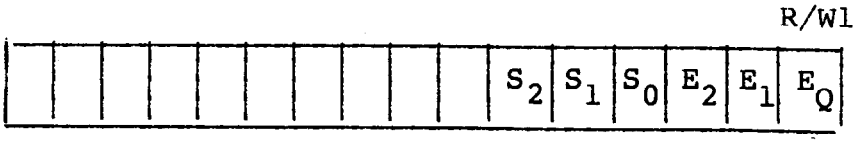
1 $\rightarrow[(A_i \cdot B_i) \cdot C_i]G_i \cdot K_i = Q_i$

2 $\rightarrow[(A_i + B_i) \cdot C_i]G_i \cdot K_i = Q_i$

3 $\rightarrow[(A_i \cdot B_i) + C_i]G_i \cdot K_i = Q_i$

4 $\rightarrow[(A_i + B_i) + C_i]G_i \cdot K_i = Q_i$

F2.A0 Reads status of enable input latch and output set



F24.A0-A2 Disable inputs on logic gates in Sections 0, 1, or 2 of the module.

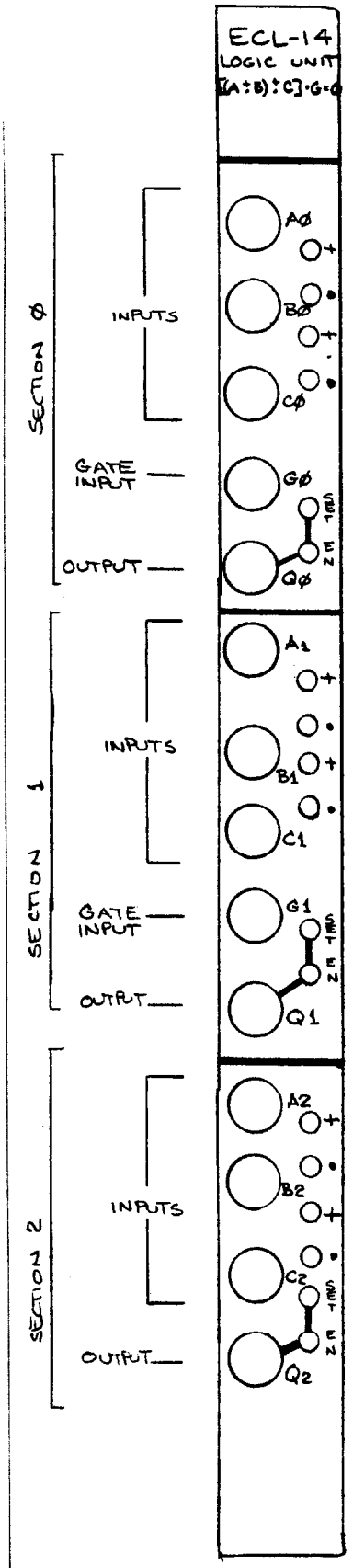
F26.A0-A2 Enable inputs on logic gates in Sections 0, 1, or 2 of the module.

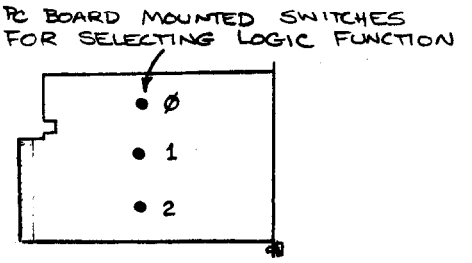
F28.A0-A2 Disable inputs on logic gates in Section 0, 1, or 2 and set ouput to a logic zero state.

F30.A0-A2 Disable inputs on logic gates in Sections 0, 1, or 2 and set output to a logic one state.

(Prepared by B. Haynes and J. Maenpaa, 8/28/78)

PANEL LAYOUT





FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	E-516	TM-0821	165

SUBJECT

DOCUMENTATION OF:

ECL-14
GENERAL LOGIC UNIT

NAME
Dave Kline

DATE	REVISION DATE
6-22-78	

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-ED-104340
FRONT PANEL MACHING DRAWING	0880-MC-104341
FRONT PANEL ASSEMBLY	0880-MC-104423
FRONT PANEL ARTWORK	0880-MC-104422
MODULE FINAL ASSEMBLY	0880-MD-104425
P.C. CARD COMPONENT ASSEMBLY	0880-MD-104424
P.C. CARD DRILL DRAWING	0880-MC-104426
P.C. CARD PARTS LIST	0880-MA-104428
P.C. CARD MASTER ARTWORK	0880-MD-104427
BOARD OUTLINE	0880-MC-104429
PHOTO REDUCTIONS	FP-33

ECL/CAMAC Module ECL-15

FAN OUT MODULE

(General Purpose Module - PC Board -

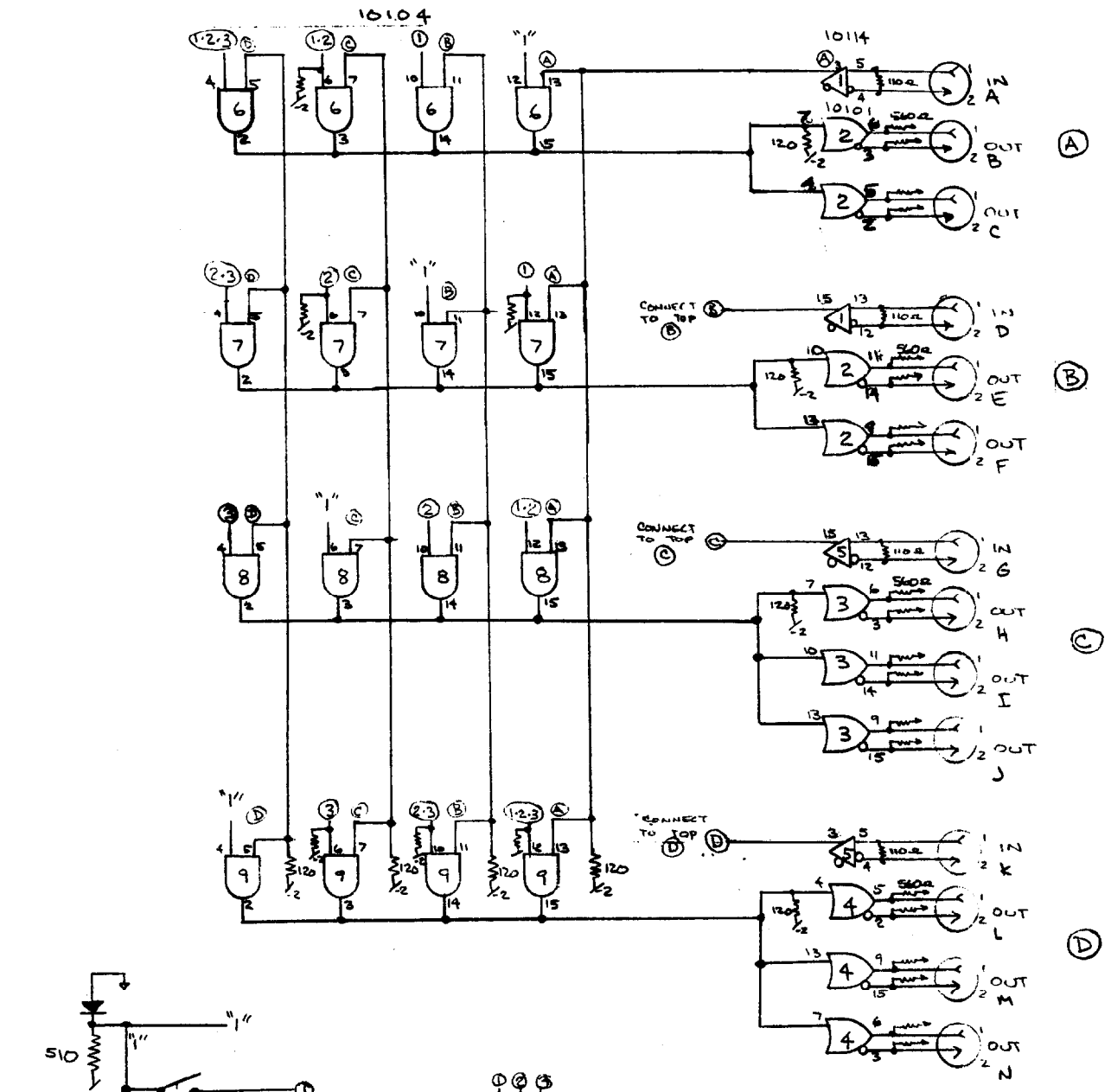
Single Width)

General Description

This provides multiple outputs for a single input. The four fan out sections (A, B, C, D) can be used independently or adjacent sections can be ORED together by setting printed circuit board switches to the desired configuration. The module can thus be used as a multiple output OR.

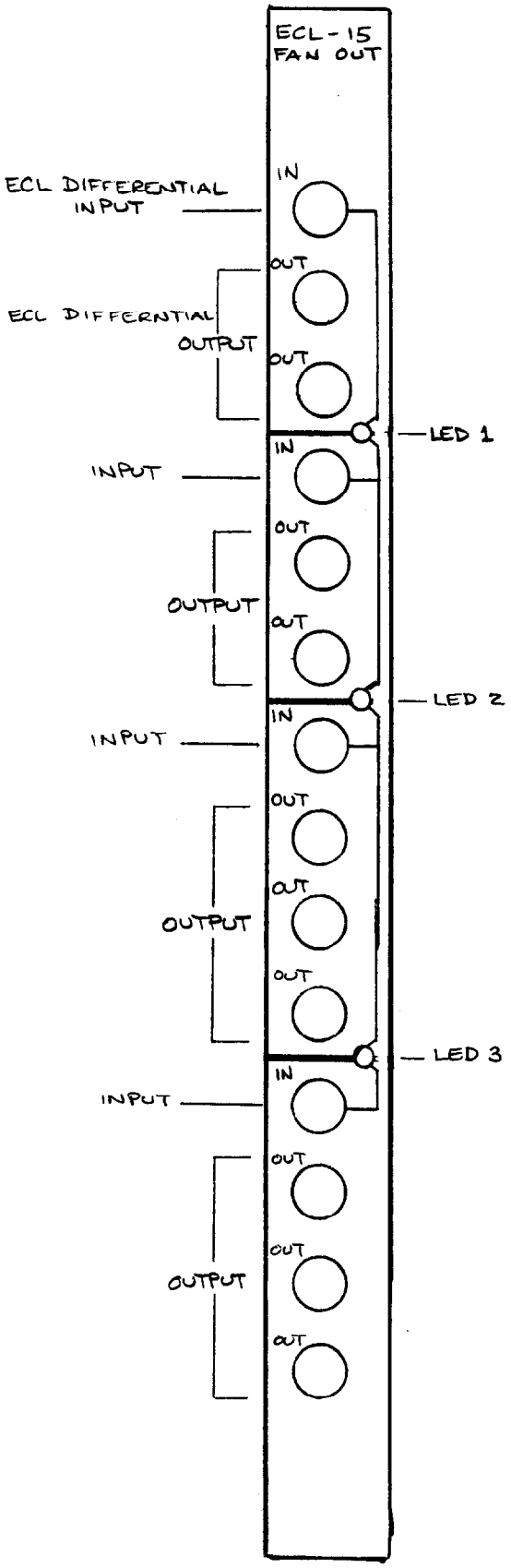
Each of the four sections has one input and two or three outputs. When the switch and the corresponding LED between two sections on the front panel are on then the inputs of those sections are ORED together.

(Prepared by J. Maenpaa and T. Soszynski, 8/28/78)



3	2	1	
0	0	0	$i \rightarrow i$ $A \cdot B \rightarrow A \cdot B$
0	0	1	$C \rightarrow C$ $D \rightarrow D$ $A \rightarrow A$ $D \rightarrow D$ $B \cdot C \rightarrow B \cdot C$ $A \cdot B \cdot C \rightarrow A \cdot B \cdot C$
0	1	0	$D \rightarrow D$ $C \cdot D \rightarrow C \cdot D$
0	1	1	$A \rightarrow A$ $B \rightarrow B$ $A \cdot B \rightarrow A \cdot B$ $C \cdot D \rightarrow C \cdot D$ $B \cdot C \cdot D \rightarrow B \cdot C \cdot D$
1	0	0	$A \rightarrow A$ $A \cdot B \cdot C \cdot D \rightarrow A \cdot B \cdot C \cdot D$
1	0	1	
1	1	0	
1	1	1	

FRONT PANEL LAYOUT



FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	Exp. 516	TM-0821	169

SUBJECT

DOCUMENTATION OF: ECL-15

NAME
H. James Krebs

DATE	REVISION DATE
6-24-78	

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-ED-104488
FRONT PANEL MACHING DRAWING	0880-MC-104489
FRONT PANEL ASSEMBLY	0880-MC-104490
FRONT PANEL ARTWORK	
MODULE FINAL ASSEMBLY	
P.C. CARD COMPONENT ASSEMBLY	
P.C. CARD DRILL DRAWING	
P.C. CARD PARTS LIST	0880-MA-104491
P.C. CARD MASTER ARTWORK	
BOARD OUTLINE	

ECL/CAMAC MODULE ECL-17

Octal Output Level Converter

(General Purpose Module - PC Board - Double Width)

1. General Description

ECL-17 consists of eight gatable, latchable signal channels that convert processor ECL signals to NIM.

The front panel, illustrated in Fig. 1 along with connector and control descriptions, is a CAMAC double width size.

Fig. 2 gives a simplified logic diagram of ECL 17; drawing 0880 ED 104495 is the complete schematic.

As illustrated in Fig. 2 the eight channel inputs require differential ECL signals. Any of these inputs left open is equivalent to a logical zero input. The outputs provide NIM logic level signals. Each output has an indicating LED which is on while an output signal is present with a minimum on time of approximately 10 milliseconds. These indicators are capable of detecting pulse widths as narrow as 2 nsec (FWHM).

There are four modes of operation:

1) Track, gated

2) Track, non-gated

3) Hold, gated

4) Hold, non-gated

These modes are switch selectable for each channel.

In the 1st mode (see Fig. 2) the latch (10130) acts as a repeater with Q=D. The input is available at the output for

PC and VALID have an on board adjustable delay of from 15 to 35 ns in 5 ns steps.

The output of the one shot is truncated by, and inhibited for the duration of, EC.

2. Specifications

2.1 Power Requirements

-5.2V at 1.4 Amps

-2V at 0.5 Amps

+6V at 20 Milliamps

2.2 Input

2.2.1 ECL

Signal levels	ECL differential
Input impedance	110 Ω differential
CMRR	±1 volt

2.2.2 NIM

Signal level	NIM, -400 mv threshold
Input impedance	50 Ω
Max input	+ 100 ma

2.3 Output

2.3.1 ECL differential open emitters with 560 Ω pull downs to -5.2 v

2.3.2 NIM (into 50 Ω)

Signal level - .72 TYP(-.7 min, -.8 max) v

4. Displays

4.1 There are 24 LED's;

8 for output signal indicators and 8 for indicating gated mode.

8 for indicating hold mode.

5. Controls

5.1 One front panel pulse duration adjustment. Continuous adjustment from 50 ns to 1000 ns.

5.2 Internal 8 station dip switch which allows selection of desired channels for gating.

5.3 Internal 8 station dip switch which allows selection of desired channels for hold mode.

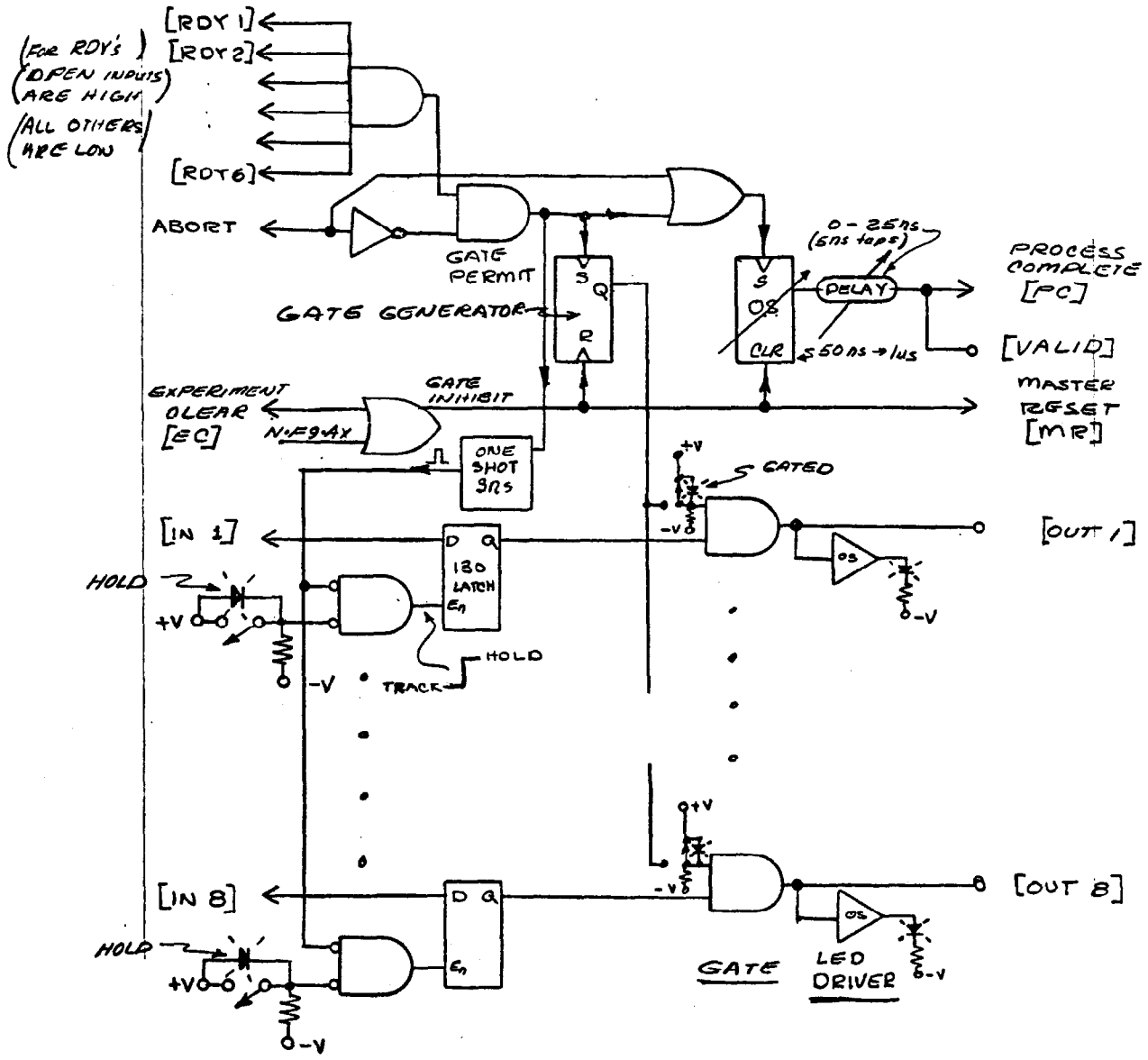
(Prepared by M. Haldeman, 10/78)

ECL-17

9-12-78

NOTES

SIGNALS ON THE LEFT ARE INPUTS
SIGNALS ON THE RIGHT ARE OUTPUTS
⟶ = DIFFERENTIAL ECL SIGNALS
o— = COAXIAL NIM SIGNALS
⊳ = EDGE TRIGGERED INPUT.
⊢ = LEVEL OPERATED INPUT OR OUTPUT



SIMPLIFIED LOGIC DIAGRAM

FIG 2

ECL/CAMAC Module ECL-19

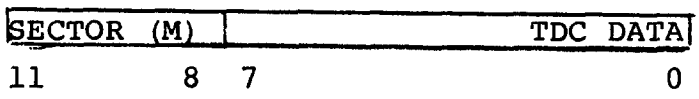
TDC Data Receiver

(Special Purpose Module - Wire Wrapped -
Double Width)

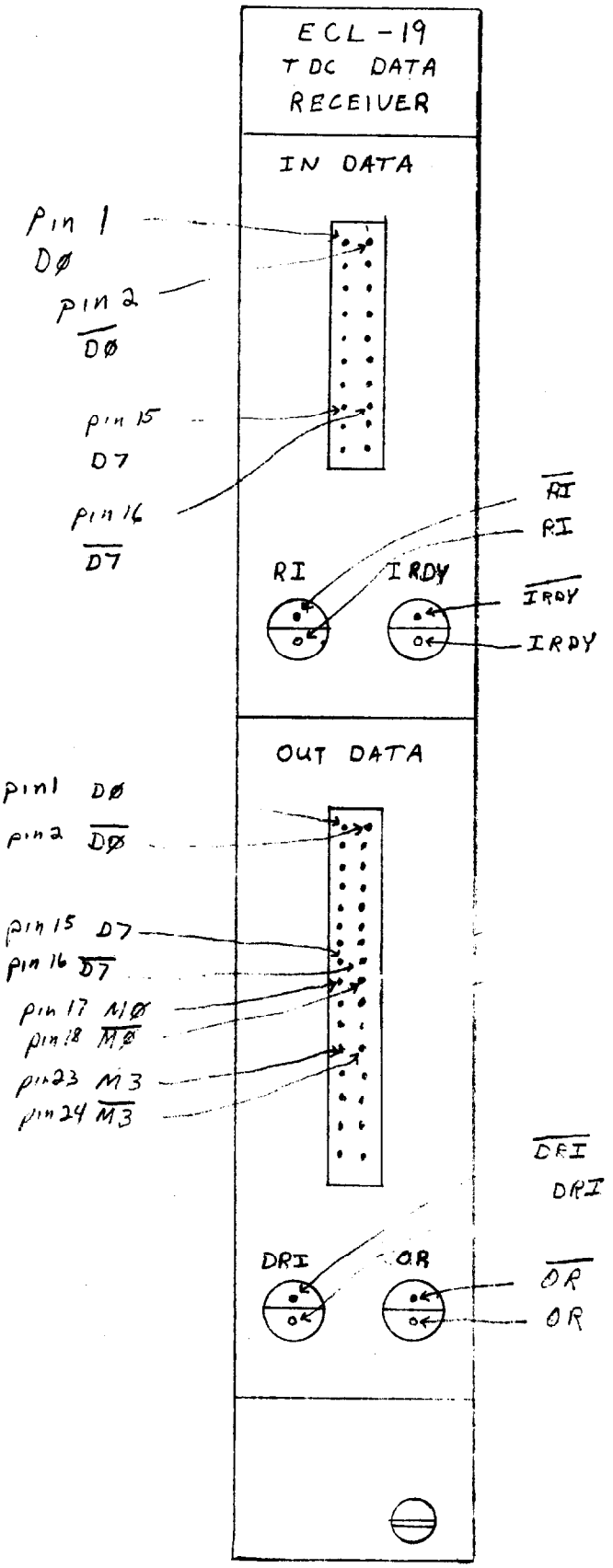
General Description

This module receives data from the ADC/TDC transmitter which segmentically transmits the data from all 15 E-516 recoil counter sectors starting with sector number 1. The module scales the number of words (M) it has received since the last reset and if the word is greater than a switch setable threshold it transmits the word and the value of M to a stack. The module must be reset after each event via the reset line on the dataway to obtain the correct value of M. The threshold value is set by an on-board octal dip switch. The switch is numbered from 1 (LSB) - 8 (MSB) and when in the on position that bit is a logical 1. All inputs and outputs are differential ECL levels. The module does not respond to any CAMAC commands.

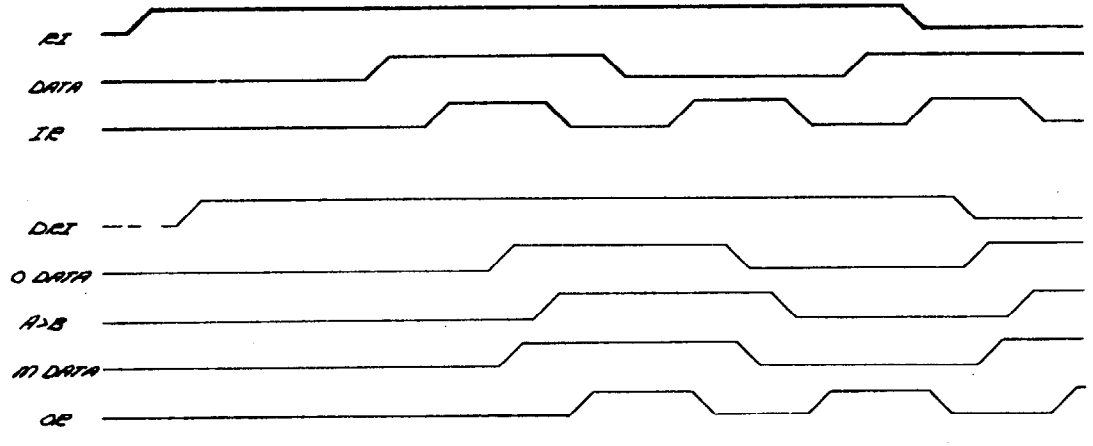
Data Output Format



K. Trepton
9/1/78



REVISIONS			
SYM	DESCRIPTION	DRAWN / APPD.	DATE / DATE



ITEM NO.	PART NO.	DESCRIPTION	Q'TY. REQ.
PARTS LIST			

UNLESS OTHERWISE SPECIFIED			ORIGINATOR: KEN JOYCE
FRACTIONS ±	DECIMALS ±	ANGLES ±	DRAWN: DALE KLINE 11-22-76
			CHECKED
1. BREAK ALL SHARP EDGES 1/64 MAX.			APPROVED
2. DO NOT SCALE DWG.			APPROVED
3. DIMENSIONING IN ACCORD WITH USASI Y14.5 STD's.			USED ON
√ MAX. ALL MACHINED SURFACES			MATERIAL-

NATIONAL ACCELERATOR LABORATORY
U.S. ATOMIC ENERGY COMMISSION

BEAM SYSTEMS
ECL-19
TIMING DIAGRAM

SCALE	FILMED	DRAWING NUMBER	REV.

FERMILAB

ENGINEERING NOTE

SECTION	PROJECT	SERIAL-CATEGORY	PAGE
BEST	Exp. 516	TM-0821	177

SUBJECT

DOCUMENTATION OF: ECL-19

NAME: H. James Krebs

DATE: 6-24-78

REVISION DATE:

DESCRIPTION	NUMBER
SCHEMATIC DIAGRAM	0880-ED-104503
FRONT PANEL MACHING DRAWING	0880-MC-104504
FRONT PANEL ASSEMBLY	0880-MC-104505
FRONT PANEL ARTWORK	
MODULE FINAL ASSEMBLY	
P.C. CARD COMPONENT ASSEMBLY	
P.C. CARD DRILL DRAWING	
P.C. CARD PARTS LIST	0880-MA-104506
P.C. CARD MASTER ARTWORK	
BOARD OUTLINE	

ECL/CAMAC Module ECL-20

16-Bit Strobed I/O MODULE

(General Purpose Test Module - Wire Wrapped - Double Width)

General Description

This module is designed to act as a test device for ECL/CAMAC modules.

The unit has a 16-bit output register and a 16-bit input register which can be written and read via CAMAC commands. The I/O registers interface to other modules via 34-pin ribbon cable connectors on the front panel. LED indicators display the register contents. An output data strobe (READY) is available via a front panel mounted 2-pin LEMO connector. Likewise an input data strobe must be provided by the module under test and brought into the input READY 2-pin LEMO on the front panel.

Output Cycle

An output cycle consists of output data becoming valid, followed by a READY strobe. An output cycle can be initiated by a CAMAC write to the output register, or by an internal clock.

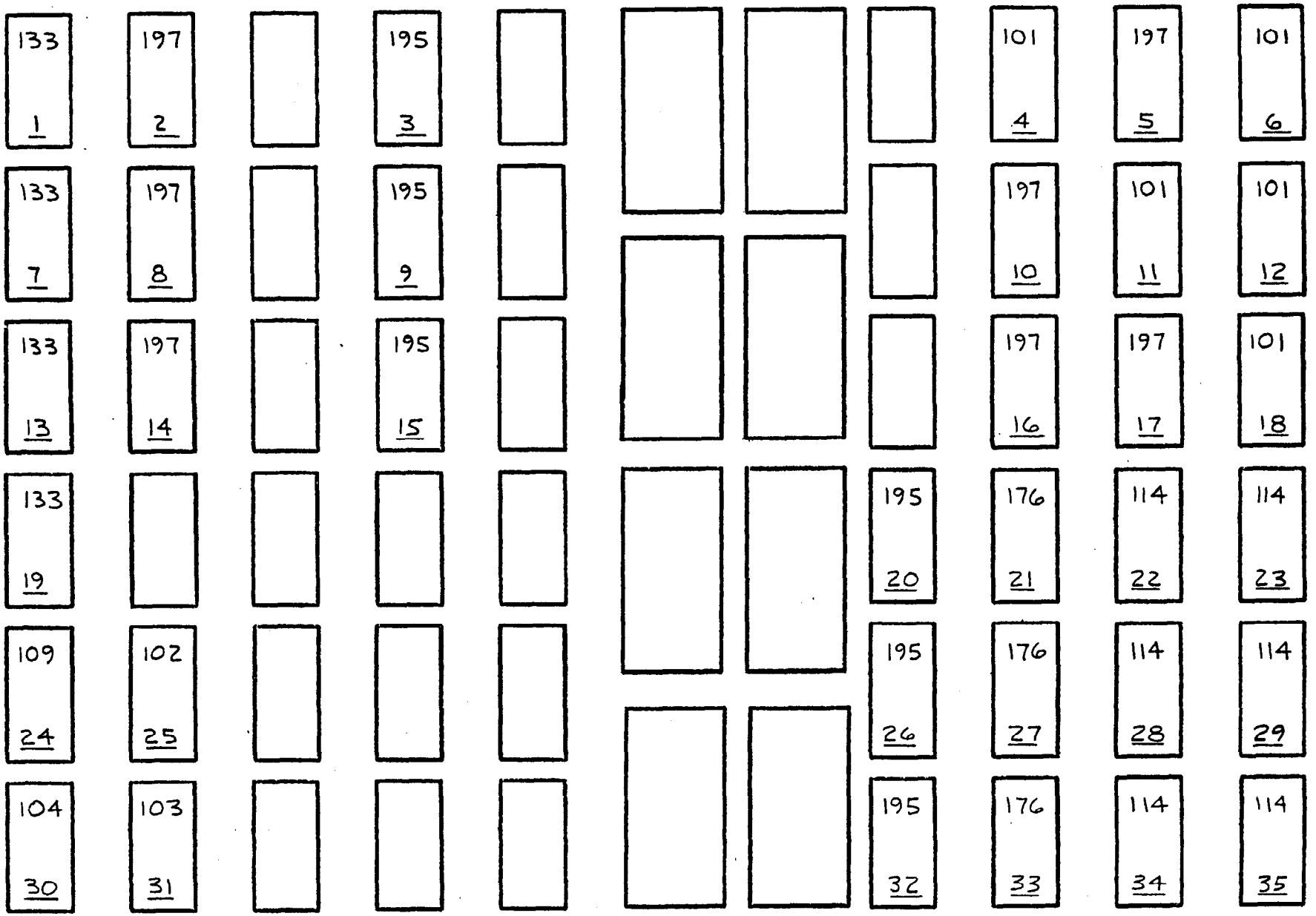
F0 A0 READ latched input register.

MSB			LSB
XXXX	XXXX	XXXX	XXXX
R/W16			R/W1

(Prepared by Rick Hance - 8/28/76)

ECL-20 PARTS LAYOUT

FRONT



ECL 10139 PROM PROGRAMMER

General Description

This unit is designed to program and read the ECL 10139 32 x 8 fusible-link PROM's. It is constructed in a 10" x 6" x 3" box and must be connected to external 24 and 5 volt power supplies.

Powering the Programmer

The unit is connected to 24 and 5 volt power supplies and the supplies are adjusted while monitoring them at the programmers test points. The device has built in diode protection against reversed power supplies so higher input voltages are required to get the proper test point voltages.

Programming PROMs

The PROM is inserted into the program socket with pin 1 toward the top. The desired address and data is set up via switches on the unit. To burn the data into the PROM, the enable button must be held down and the program button momentarily depressed. The duration of the programming pulse is internally controlled and a LED indicator next to the programming button will flash during the cycle.

This process is completed until all desired locations are programmed. Zeroes will remain in all unprogrammed locations.